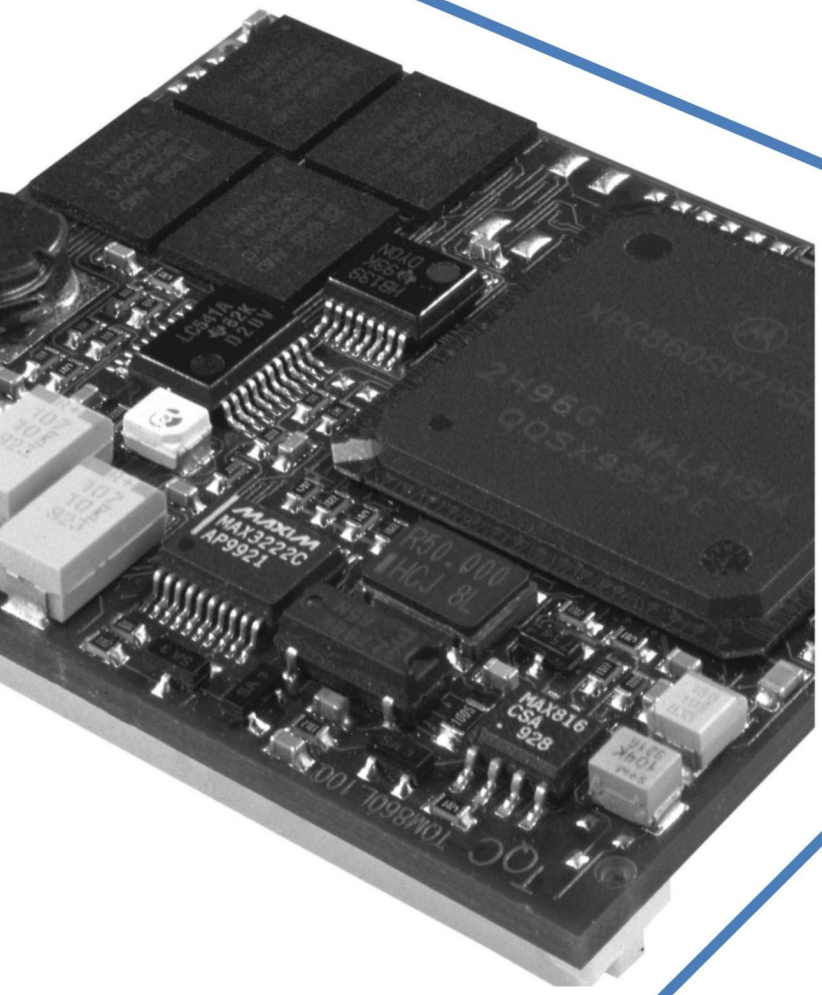
The key
to the embedded world



TQM8xxL Hardware Manual

1 About This Manual

This document encompasses the technical features of various Microcontroller-modules of the TQM8xxL family. The name MPC860 is often used synonymously for all Microcontrollers of the MPC8xx family. Similarly, TQM860L refers, in most cases, to all variants listed in **Illustration 4-1: Variant Codes**.

©2004 by TQ-Components GmbH

1.1 Terms and Conventions

Symbol/Tag	Description
	This symbol represents the handling of electrostatic - sensitive modules and/or components. These components are often damaged/destroyed with the transmission of a voltage higher than about 50V. Human body usually notices electrostatic discharges only above approximately 3,000V.
	This symbol indicates the possible use of voltages greater than 24V. Please note the relevant statutory regulations in this regard. Non-compliance with these regulations can lead to serious damage to your health and also cause damage/destruction of the component.
	This symbol indicates the possible source of danger. Acting against the procedure described can lead to possible damage to your health and/or cause damage/destruction of the material used.
	This symbol represents important details or aspects for working with TQ products.
Filename.ext	This specification is used to state the complete file name with its corresponding extension.
Instructions / Examples	Examples of application. e.g. • Specifying memory partitions • Processing a script • .....
Reference	Cross-reference to another section, figure or table.

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

1.2 Table of Contents

1	About This Manual	2
1.1	Terms and Conventions	3
1.2	Table of Contents	4
1.3	List of Figures / Table Overview	6
1.4	Acronyms and Definitions	7
1.5	Tips on Safety	7
1.6	Handling/ESD Tips	8
1.7	Registered Trademark	8
1.8	Imprint	9
1.9	Copyright	9
1.10	Limited Liability	9
1.11	Revision History	9
2	Introduction	10
2.1	Scope of Supply	11
2.2	First Steps	13
2.2.1.	Board Setup	13
2.2.2.	Downloading the Demo Application	17
3	Technical Specification	20
3.1	Electronic Specification	20
3.1.1.	Block Diagram	20
3.1.2.	System Components	20
3.1.2.1	CPU	21
3.1.2.2	Permanent Memory (Flash)	21
3.1.2.3	Synchronous Dynamic Random Access Memory (SDRAM)	23
3.1.2.4	CAN Controller	23
3.1.3.	Bus Driver	25
3.1.3.1	CPU Clock	25
3.1.3.2	RTC Pulse	26
3.1.3.3	CAN Pulse	27
3.1.4.	Reset Behavior	27
3.1.4.1	Reset Configuration	27
3.1.4.2	Reset Logic	30
3.1.4.2.1	Tolerances and Reset Thresholds for VCC3V3	30
3.1.4.2.2	Tolerances and Reset Threshold for VCC5V	32
3.1.4.2.3	External Reset Input	32
3.1.5.	Power Supply (with different possibilities of the supply)	33
3.1.5.1	Possibilities of Power Supply	33
3.1.5.2	3,3V Supply	33
3.1.5.2.1	Current Consumption at 3,3V	34
3.1.5.3	Regulator for 3,3 V	34
3.1.5.4	5V Power Supply	35
3.1.5.5	Current Consumption from 5 V Direct	35
3.1.5.6	Total Consumption at 5 V	36
3.1.5.7	Battery Buffering	36
3.1.6.	Interfaces	37
3.1.6.1	Serial Interfaces	37
3.1.6.2	Download Interface	37
3.1.6.3	BDM Interface	38
3.1.7.	Module connector	39
3.1.7.1	Pin Assignment	39
3.2	Mechanical Specification	48
3.2.1.	General Information	48

©2004 by TQ-Components GmbH

3.2.2.	Dimensions	48
3.2.3.	Connector	50
3.2.4.	Tips on handling	50
4	Variant codes	51
5	Environmental Conditions	53
5.1	Climatic Conditions and Areas of Application	53
5.2	Installation Instructions	53
5.3	Reliability and Life-span	53
5.4	Product Qualification	53
5.4.1.	Mechanical Environmental Influences	53
5.4.2.	Temperature Tests	54
5.4.3.	EMI/EMC	54
5.4.4.	EMC Passive / Radiation	54
5.4.5.	ESD	54
5.4.6.	UL Approval	54
6	Safety requirements and Personnel Protection	54
6.1	EMI/EMC Requirements	54
6.2	ESD Requirements	55
6.3	Operational Safety and Personnel Protection	55
7	Annexure	56
7.1	Software Support	56
7.1.1.	Monitor Software	56
7.1.2.	Configuration of the SDRAMs	57
7.1.3.	Configuration of the CAN Controller	62
7.2	Tools	65
7.2.1.	Starter Kit STK8xxL	65
7.2.2.	Module Extraction Tool MOZI8xxL	67
7.3	Circuit Diagrams	68
7.3.1.	Starter Kit	68
7.3.2.	FETH8xxL	75
7.4	Literature	77

©2004 by TQ-Components GmbH

1.3 List of Figures / Table Overview

Illustration 1-1: Terminology 7
Illustration 1-2: Revision History 9
Illustration 2-1: TQM8xxL 10
Illustration 2-2: The Tera Term: Serial Port dialog box is displayed. 14
Illustration 2-3: The Tera Term: Serial Port setup 15
Illustration 3-1: Block Diagram 20
Illustration 3-2: Command Sequence for programming a 32-bit word 22
Illustration 3-3: SDRAM Programming 23
Illustration 3-4: Mapping the CAN Controller 24
Illustration 3-5: Bus Structure 25
Illustration 3-6: Clock frequencies 26
Illustration 3-7: Tolerance RTC-Pulse 26
Illustration 3-8: Tolerance CAN Pulse 27
Illustration 3-9: Reset Configuration 29
Illustration 3-10: Tolerances of 3,3V supply, standard temperature range 31
Illustration 3-11: Tolerances of 3,3V supply, extended temperature range 31
Illustration 3-12: Structure of the power supply 33
Illustration 3-13: 3,3V Supply 33
Illustration 3-14: Current consumption at 3,3V 34
Illustration 3-15: 5V Supply 35
Illustration 3-16: Current Consumption from 5V direct 35
Illustration 3-17 Total Consumption at 5V 36
Illustration 3-18: Battery Buffering 36
Illustration 3-19: Driver structure of the RS232 interfaces 37
Illustration 3-20: Signals of the download interface 37
Illustration 3-21: Signals of the BDM interface 38
Illustration 3-22: Pin assignment 47
Illustration 3-23 Top view of the PCB 49
Illustration 3-24: PCB heights (not to scale) 49
Illustration 3-25: Overview of Connector 50
Illustration 4-1: Variant Codes 51
Illustration 4-2: Standard Types of Modules 52
Illustration 7-1: Initializing SDRAM 60
Illustration 7-2: Single read Burst read SDRAM 61
Illustration 7-3: Single write and burst write SDRAM 61
Illustration 7-4: Refresh and Exception SDRAM 62
Illustration 7-5: Configuration of CAN Controllers 63
Illustration 7-6: Single read and burst read CAN 64
Illustration 7-7: Single write and burst write CAN 64
Illustration 7-8: Refresh and Exception CAN 65
Illustration 7-9: Starter Kit 65
Illustration 7-10: Standard types of the starter kit 67
Illustration 7-11: Module Extraction Tool 67

©2004 by TQ-Components GmbH

1.4 Acronyms and Definitions

The following terminology and abbreviations are used:

Acronym	Full Form
BDM	Background Debug Mode
CPU	Central Processing Unit
CAN	Controller Area Network
EEPROM	Electrically Erasable Programmable Read-Only Memory (Byte wise re-writable)
EMI / EMC	Electro Magnetic Interference / Electro Magnetic Compatibility
Flash	Electrically Erasable Programmable Read-Only Memory (Block Erase)
JTAG	Joint Test Action Group
MCU	Memory Control Unit
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SMD	Surface Mounted Device

Illustration 1-1: Terminology

1.5 Tips on Safety

Improper or incorrect handling of the product can substantially reduce its life span.

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

1.6 Handling/ESD Tips

General handling of your TQ products

The handling and use of your TQ product may be done exclusively by qualified personnel.

Ensure that while using your TQ product, particularly while plugging in/out of modules, changing jumper settings, or connecting other external devices, the power supply is not connected to your TQ product. Violation of this guideline can result in damage/destruction of the module and cause danger to your health.

Improper handling of your TQ product would render the guarantee invalid.

Proper ESD handling

The ESD components must be used in workplaces which are apt for the handling them in order to avoid damage or destruction.

1.7 Registered Trademark

The TQ-Components GmbH has strived to observe the copyright of the graphics and texts used in all publications, and to use those created by them or those, which are license-free.

All brand names and trademarks contained in this publication are protected by copyright, unless specifically stated otherwise, of the corresponding owner or holder of the same. The sheer mention cannot be used to conclude that brand names and registered trademarks are not copy protected by third parties.

©2004 by TQ-Components GmbH

1.8 Imprint

TQ-Components GmbH
Schulstrasse, 29 D
82234 Wessling
Tel : +49/(0) 8153/9308-333
Fax : +49/(0) 8153/9308-134
Email : info@tqc.de
Web : http://www.tq-components.com

1.9 Copyright

Copyright protected © 2004 by TQ-Components GmbH.
This handbook may not be copied, reproduced, translated, restructured or distributed, either in whole or in part, in electronic, machine-readable or other form, without the explicit written consent of TQ-Components GmbH.

1.10 Limited Liability

The TQ-Components GmbH does not take over any guarantee for the currentness, correctness or quality of the information provided in this manual as also its further use. Claims lodged against TQ-Components GmbH, related to damages of material or intellectual nature, arising out of the use or non-use of information contained in this manual, or out of the use of incorrect or incomplete information, would not be entertained so long as there is no evidence of intentional or negligent fault on the part of TQ-Components GmbH.

The TQ-Components GmbH reserves the right to change or amend the contents of this manual or parts thereof without prior notice.

1.11 Revision History

Revision (Version) History					
		Created		Approved	
Rev	Modification	Date	Cipher	Date	Cipher
300	Creation	2004/11/24	NIS	2004/12/06	ANW

Illustration 1-2: Revision History

2 Introduction

The TQM8xxL is a universal Minimodule, equipped with the PowerPC - CPU MPC8xx of Freescale (Semiconductor). Its dimension is 40×54 mm², approximately half the size of a credit card. The TQM8xxL represents a very compact, powerful and universally applicable computer core, which can sustain harsh industrial environments.

Illustration 2-1: TQM8xxL

The pin assignment is compatible with one another for all modules of the TQM8xxL family. Thus, for example, the pins of the TQM860L are a superset of the pins of the TQM850L. In this manner, based on the requirements, modules with different computing capabilities and interfaces can be used on a main board.

All relevant pins of the microprocessor, particularly all the port pins, are brought out on the connector. With this, the system on the baseboard becomes transparent for the developer, and all possibilities of the Hardware can be tapped to the full extent.

In particular, the following facts contribute to the good industrial suitability of the module:

- SMD population on both sides
- Memory securely soldered on the board (Flash and SDRAM)
- Small PCB height effecting good mechanical characteristics (mechanical vibration and shock).
- Robust plug-in system with a lead wire spacing of 0,8 mm
- Single-source voltage supply of 5V

©2004 by TQ-Components GmbH

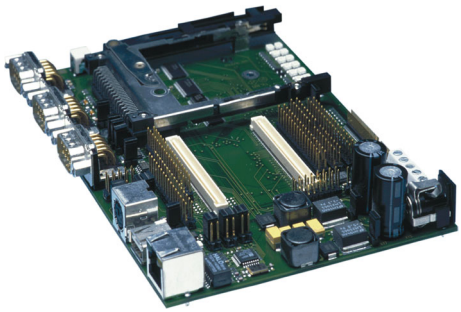
Short commissioning times of a newly developed system can be achieved by using the starter kit ("Plug and Play"). Time-consuming wired board development prototypes for commissioning the processor are eliminated, and the first taste of success is achieved in just a few minutes.

2.1 Scope of Supply

The following items are included in your starter kit box:

Module TQM8xxL

Starter kit STK8xxL



Power Supply

TQM8xxL.HWM.0300.doc

©2004 by TQ-Components GmbH

Download cable

Tool CD

©2004 by TQ-Components GmbH

2.2 First Steps

2.2.1. Board Setup

Your STK8xxL is already configured for the module desired by you. Note that all names of connectors refer to those of the starter kit. The circuit diagrams of the starter kit are given in section 7.3.1 Circuit diagrams Starter kit.

! note !	For further information on the starter kit STK8xxL please refer to the enclosed hardware manual for the starter kit.

1. **Power supply**

X16: Closing the jumper X16 activates the 3,3V supply to the starter kit. If your TQM8xxL has no DC converter then this jumper must be closed.

X17: Closing the jumpers X17 activates the 5V supply to the starter kit. This jumper must always be closed in order to ensure that the available interfaces are operational.

2. **ENMON Circuit:** The ENMON circuit can be activated by closing the jumper X34 so that during operation of the board commands can be sent and received via the serial interface.

3. **Activate LEDs:** In order to ensure that the LEDs V16-V31 can be activated, close the jumper X33.

In order to check the configuration of the starter kit, please proceed as follows:

1. Start your PC. Install the terminal program “Tera Term Pro” from the Tool CD on your PC.

2. Start the program Tera Term.

3. Select **Serial port** from the **Setup** Menu.

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

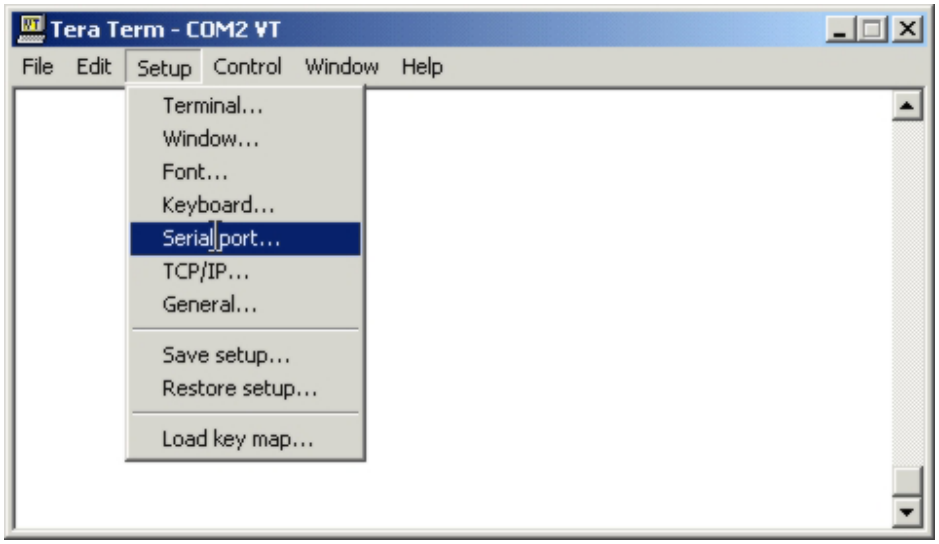


Illustration 2-2: The Tera Term: Serial Port dialog box is displayed.

Set the required parameters

Port:	**COMx** (Set the port of the serial interface used on the PC)
Baud rate:	**38400** (transmission speeds up to 115200 can be implemented, we recommend 38400)
Data:	**8 bit**
Parity:	**none**
Stop:	**1 bit**
Flow Control:	**Xon/Xoff**

©2004 by TQ-Components GmbH

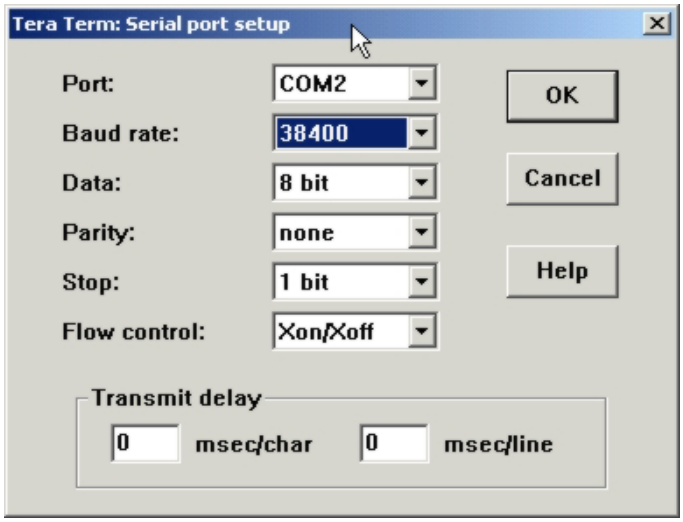
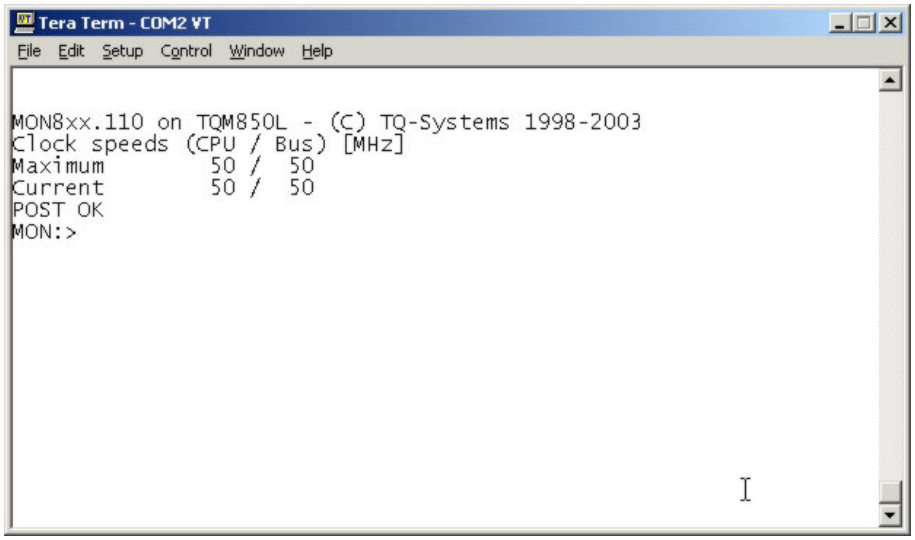


Illustration 2-3: The Tera Term: Serial Port setup

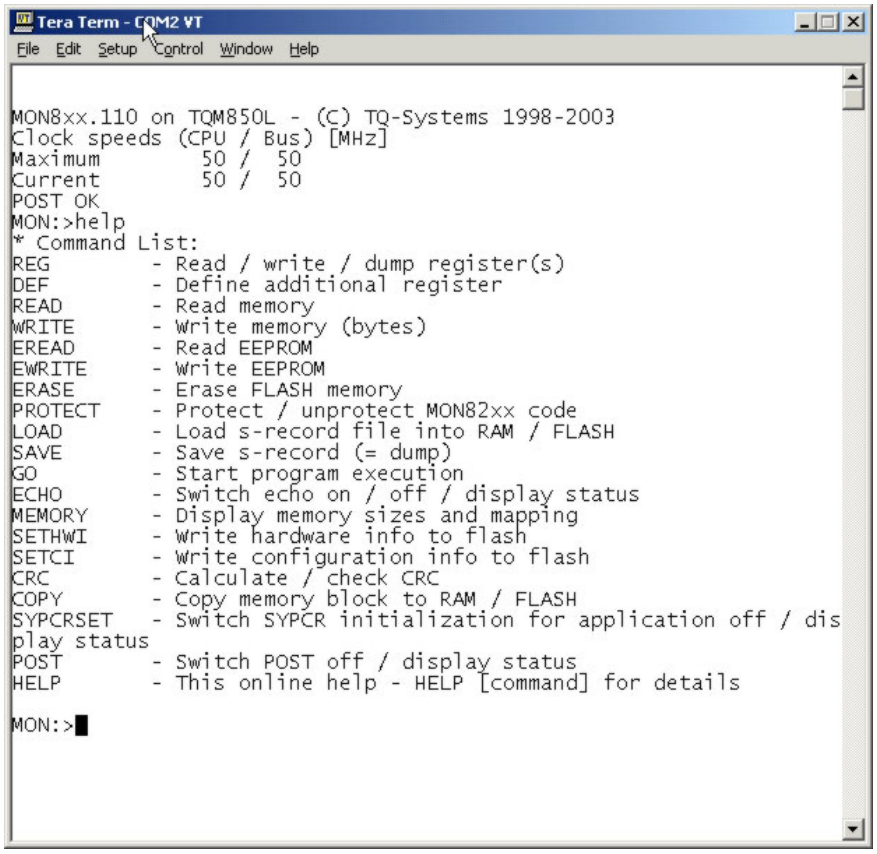
! note !	The pre-requisite of the terminal program Tera Term Pro is that the Operating System of your PC is compatible with MS-Windows. For other Operating Systems (e.g. Linux) please use the appropriate alternatives.

4. Connect the serial interface of your PC with the connector X19 of your starter kit using the download cable.
5. Switch on the board using the adaptor.
6. Press the Reset button S1 on your starter kit.
7. Press the key **Enter** 5 times on your PC. The module responds via the serial interface.

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH


Tera Term - COM2 VT
File Edit Setup Control Window Help
MON8xx.110 on TQM850L - (C) TQ-Systems 1998-2003
Clock speeds (CPU / Bus) [MHz]
Maximum 50 / 50
Current 50 / 50
POST OK
MON:>

8. Enter the command **help** in order to get a list of the available commands.


Tera Term - COM2 VT
File Edit Setup Control Window Help
MON8xx.110 on TQM850L - (C) TQ-Systems 1998-2003
Clock speeds (CPU / Bus) [MHz]
Maximum 50 / 50
Current 50 / 50
POST OK
MON:>help
* Command List:
REG - Read / write / dump register(s)
DEF - Define additional register
READ - Read memory
WRITE - Write memory (bytes)
EREAD - Read EEPROM
EWRITE - Write EEPROM
ERASE - Erase FLASH memory
PROTECT - Protect / unprotect MON82xx code
LOAD - Load s-record file into RAM / FLASH
SAVE - Save s-record (= dump)
GO - Start program execution
ECHO - Switch echo on / off / display status
MEMORY - Display memory sizes and mapping
SETHWI - Write hardware info to flash
SETCI - Write configuration info to flash
CRC - Calculate / check CRC
COPY - Copy memory block to RAM / FLASH
SYPCRSET - Switch SYPCR initialization for application off / dis
play status
POST - Switch POST off / display status
HELP - This online help - HELP [command] for details
MON:>

©2004 by TQ-Components GmbH

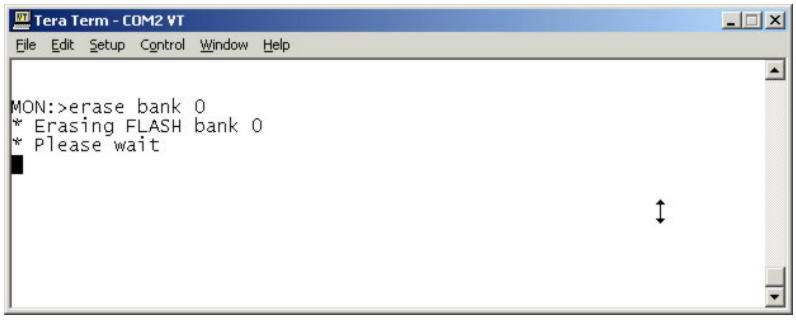
! note !

For further information on the MON8xx monitor program please refer to the enclosed software manual.

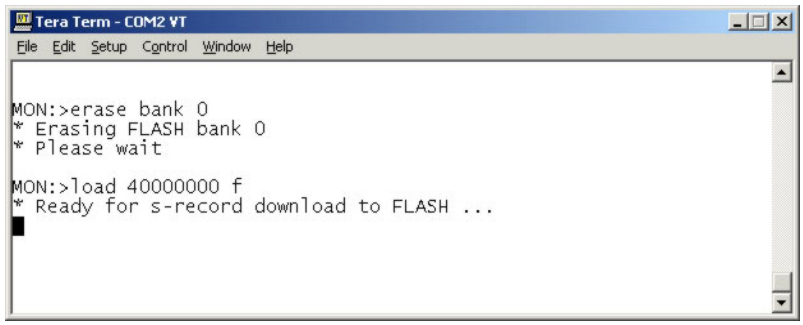
2.2.2. Downloading the Demo Application

The prerequisite for this step is that a functional communication link should have been established via the serial interface (refer to 2.2.1).

1. Erase the Flash Bank 0 by entering the command erase bank 0.



2. Load the Demo file in the Module by entering the command load **40000000 f**

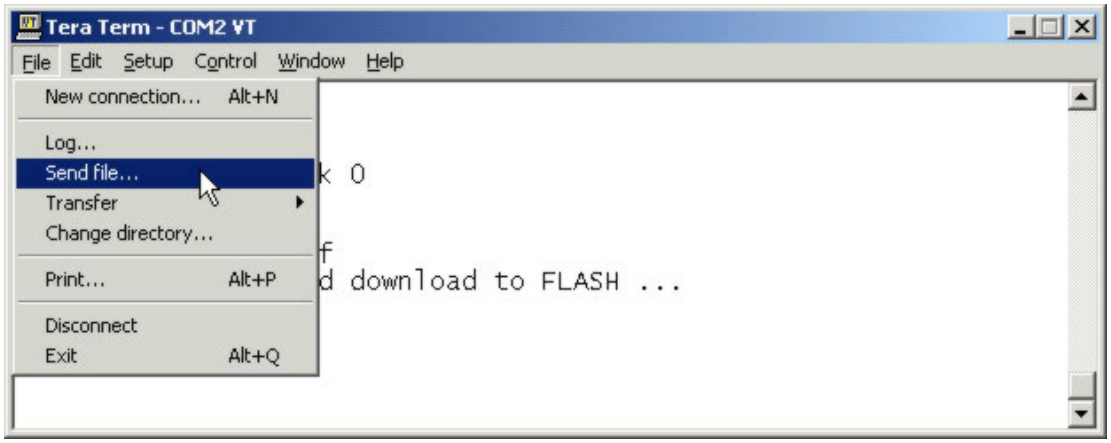

Tera Term - COM2 VT
File Edit Setup Control Window Help
MON:>erase bank 0
* Erasing FLASH bank 0
* Please wait
MON:>load 40000000 f
* Ready for s-record download to FLASH ...

! note !

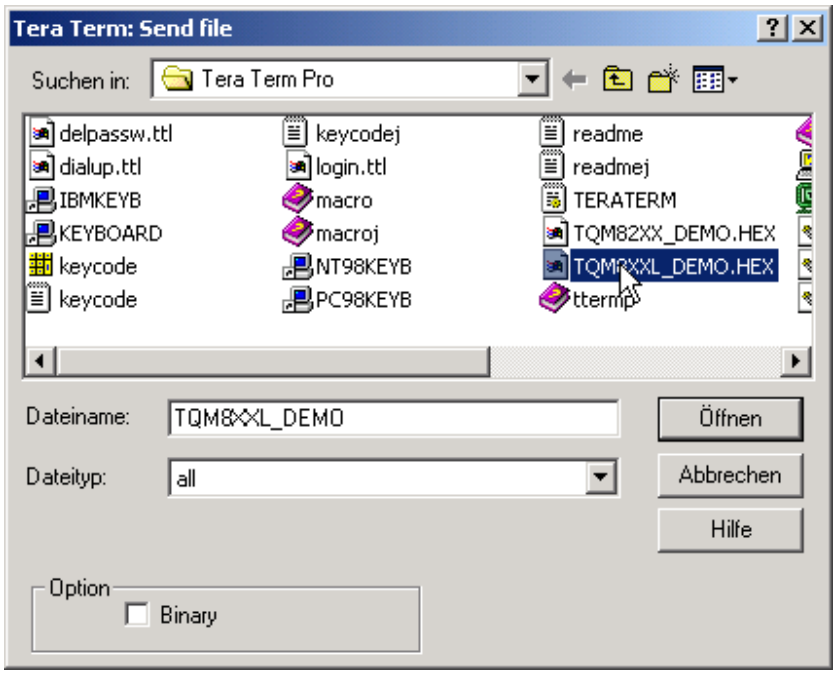
The time required to delete the flash memory is between a few seconds to a few minutes depending on the memory area to be deleted.

©2004 by TQ-Components GmbH

Select **Send File** from the **File** menu.

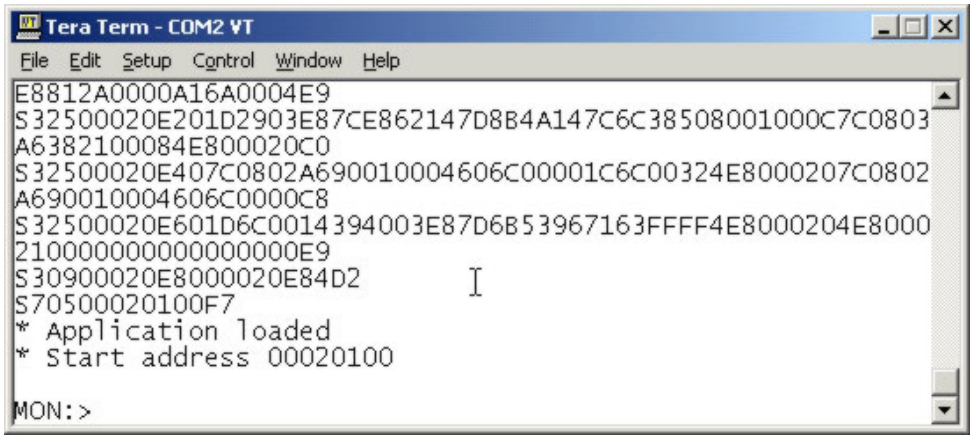


Select the file ***TQM8xxL_DEMO.hex***. You will find this on your Tool CD.



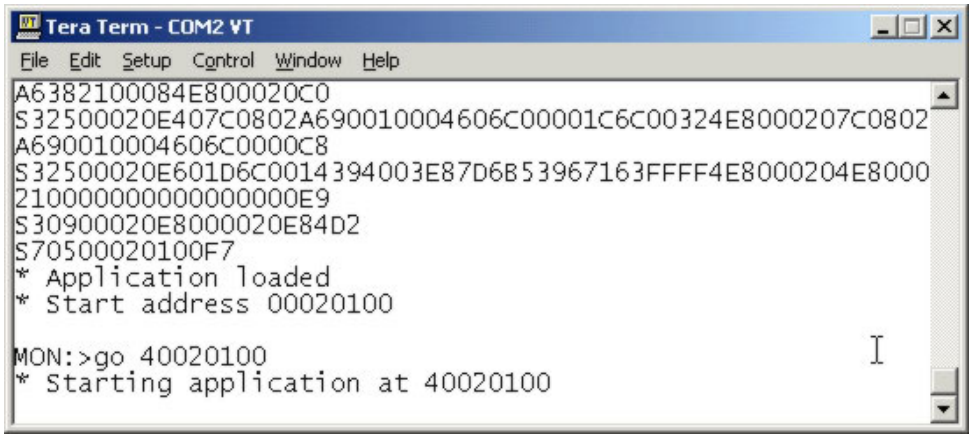
The Demo application is transferred on to the module.

©2004 by TQ-Components GmbH



After the download the relative start address **00020100** of the application is output. Please note that an offset of **40000000** has to be added, which yields the start address **40020100**.

Start the Demo application by entering the command **go 40020100**



You can check the correct functioning of the program by means of the lighting sequence on the LEDs V16-V31 of the starter kit.

©2004 by TQ-Components GmbH

3 Technical Specification

3.1 Electronic Specification

3.1.1. Block Diagram

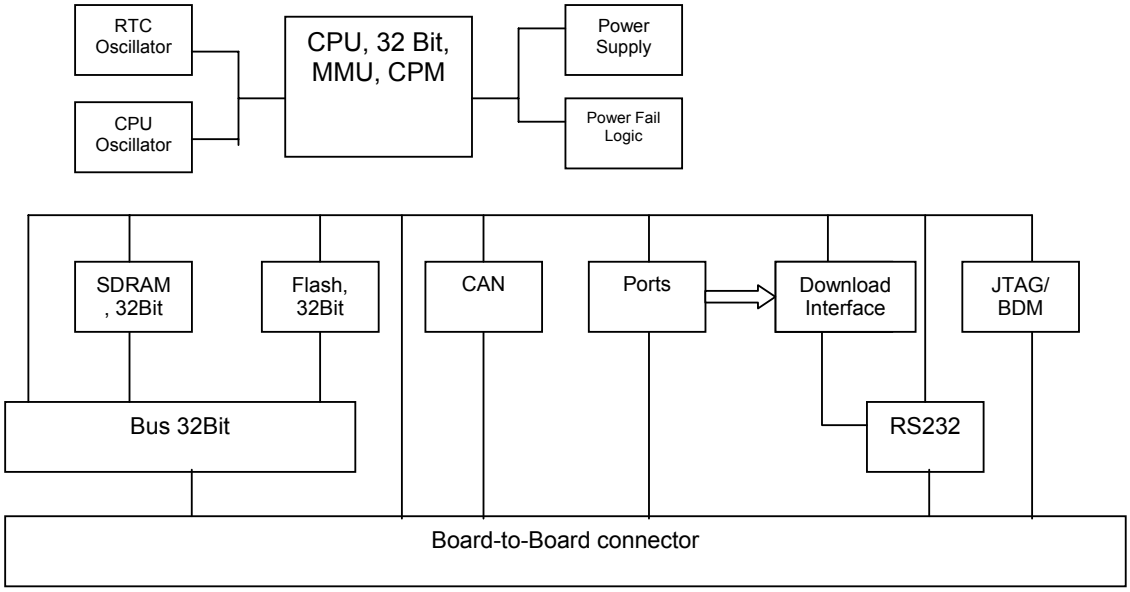


Illustration 3-1: Block Diagram

3.1.2. System Components

- CPU MPC8xx
- Oscillator for the CPU
- Oscillator for the RTC
- Power-fail Logic
- DC/DC converter
- SDRAM
- Flash
- 2 * Full CAN 2.0 B active controller
- 2 * RS232 serial driver for SMC1 and SMC2
- BDM / JTAG Interface
- Board-to-Board connector system, 240 Pins, lead wire spacing 0,8 mm

©2004 by TQ-Components GmbH

3.1.2.1 CPU

The module has been developed for the MPC860, however, even an MPC855, MPC850 or MPC823 can be used. Subject to adequate product qualification, future derivatives could also be used as long as they are functionally compatible with the MPC860.

> **! note !** The addresses for the control of the SDRAMs are multiplexed internally. Hence an external bus master can not be connected to the bus (e.g. PCI bridge, Multiprocessor system).

3.1.2.2 Permanent Memory (Flash)

16 bit 3,3V Flashes with BGA packages are used. These are controlled directly by the CPU without a driver/buffer.

- 4 to 8 MB
- 1 or 2 banks with 32 bit
- Access time 90ns
- Signals used:

  CS_FLASH0#/CS0# (bootable) and if available CS_FLASH1#/CS1#, OE#/GPL_AB1#, WE0#/BS_B0#, WE2#/BS_B2#
- Control via GPCM, recommended timing:
  ACS = 00, TRLX = 0, CSNT = 1, SCY = 4, EHTR = 1 (Normal operation),
  ACS = 11, TRLX = 1, CSNT = 1, SCY = 15, EHTR = 0 (Boot mode)

The address lead A29 (Bit 31 is the least significant address lead!) is connected with A0 of the Flash because of which the addresses, and the command sequences have to be shifted left by two bits while programming or deleting, i.e. multiplied by four.

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

Example: Command sequence to program a 32-bit word

	1. Bus cycle		2. Bus cycle	
	Address	Data	Address	Data
Specification AMD	0x0555	0x00AA	0x02AA	0x0055
TQM860L	0x40001554	0x00AA00AA	0x40000AA8	0x00550055
	3. Bus cycle		4. Bus cycle	
	Address	Data	Address	Data
Specification AMD	0x0555	0x00A0	PA	32 Bit Data
TQM860L	0x40001554	0x00A000A0	PA	32 Bit Data

Illustration 3-2: Command Sequence for programming a 32-bit word

The address to be programmed is identical in both cases.

The status signal RY/BY# of the Flash is not used, i. e. the execution of the write and delete cycles must be monitored by polling the Flash status bits (DQ7#, Toggle Bits etc.) [4].

Since each of the two 16 bit Flashes of a 32-bit bank has only one write-enable signal, only 16 or 32 bits can be written (programmed). Individual bytes can be programmed as follows:

1. Read the data word from the Flash, which contains the byte to be programmed.
2. Replace the byte to be programmed in the data word.
3. Write the data word back into the Flash.

©2004 by TQ-Components GmbH

3.1.2.3 Synchronous Dynamic Random Access Memory (SDRAM)

16-bit SDRAM modules are used in the TSSOP54 housing.

- 16 - 64 MB
- 1 memory bank with 32 bit
- Clock 50 MHz (50 MHz module), 66 MHz (66 MHz module) or 40 MHz (80 MHz module)
- Signals used:

CS_SDRAM0#/CS2#	
GPL_AB0#	(A10 SDRAM)
OE#/GPL_AB1#	(WE# SDRAM)
GPL_AB2#	(RAS# SDRAM)
GPL_AB3#	(CAS# SDRAM)
BS_A0#	(DQMU SDRAM, Bits 0 .. 7)
BS_A1#	(DQML SDRAM, Bits 8 .. 15)
BS_A2#	(DQMU SDRAM, Bits 16 .. 23)
BS_A3#	(DQML SDRAM, Bits 24 .. 31)
CLKOUT	
CKE	(only foreseen with Pull-up)

- Control and refresh via UPMA
- CAS Latency 2

Depending on the memory capacity 2 chips each of 16, 64, 128 or 256 MBit are used.

The following access schematic is recommended (refer to [5] Literature):

CLKOUT	Single Read	Burst Read	Single Write	Burst Write	SDRAM type
66 MHz	4 + 1	4 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1+ 1	PC133
50 MHz	4 + 1	4 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1+ 1	PC100
40 MHz	4 + 1	4 + 1 + 1 + 1 + 1	3 + 1	3 + 1 + 1 + 1+ 1	PC100

Illustration 3-3: SDRAM Programming

3.1.2.4 CAN Controller

Either one or two AS82527 (Intel) are used. These are controlled by the CPU using the driver (Addresses, Chip Select) and buffer (Data).

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

- Two fully compatible CAN 2.0b interfaces
- No CAN driver (inputs and outputs at TTL level)
- Clock pulses from the common 16 MHz Quartz on the first controller, CLKOUT of the first controller is connected to XTAL1 of the second
- Accesss mode 8 bit non-multiplexed
- Signals used:

  CS_CAN#/CS3#
  GPL_AB2# (R/W# CAN)
  GPL_A5# (Buffer Enable Bus Transceiver for CAN)
  A22, A23 (Address decoding)
  HRESET# (RESET# CAN)
  IRQ_CAN#/IRQ4# (common Interrupt for CAN)

- Control via UPMB, adaptive timing (Wait Signal)
- Recommended settings: Refer to [6] Literature

The resultant mapping, with respect to the base address of CS_CAN#/CS3#, is as illustrated in Illustration 3-4: Mapping the CAN **Controller**. The area shown is shadowed at the offsets +0x400, +0x800 etc. Access to the area 0x200 up to 0x3FF and their shadows lead to a Bus Timeout and should be avoided.

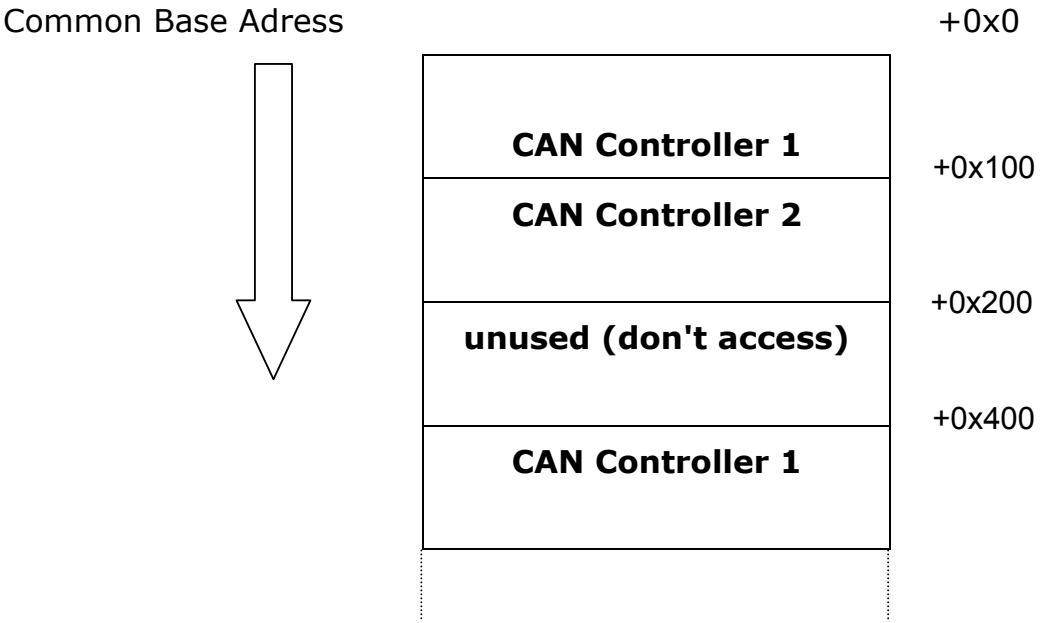


Illustration 3-4: Mapping the CAN Controller

©2004 by TQ-Components GmbH

3.1.3. Bus Driver

- No buffering of the address leads on the module: The SDRAM and Flash are driven without additional delays.
- Unbuffered address bus brought out: External peripherals can be connected by first switching on a driver. The load capacity required for a driver input is available.
- Unbuffered data bus brought out: Direct connection up to about 20 pF is possible; beyond that external buffers would be necessary.

! note ! In order to avoid conflicts with the Reset configuration, buffers with "Bus Hold" may not be used.

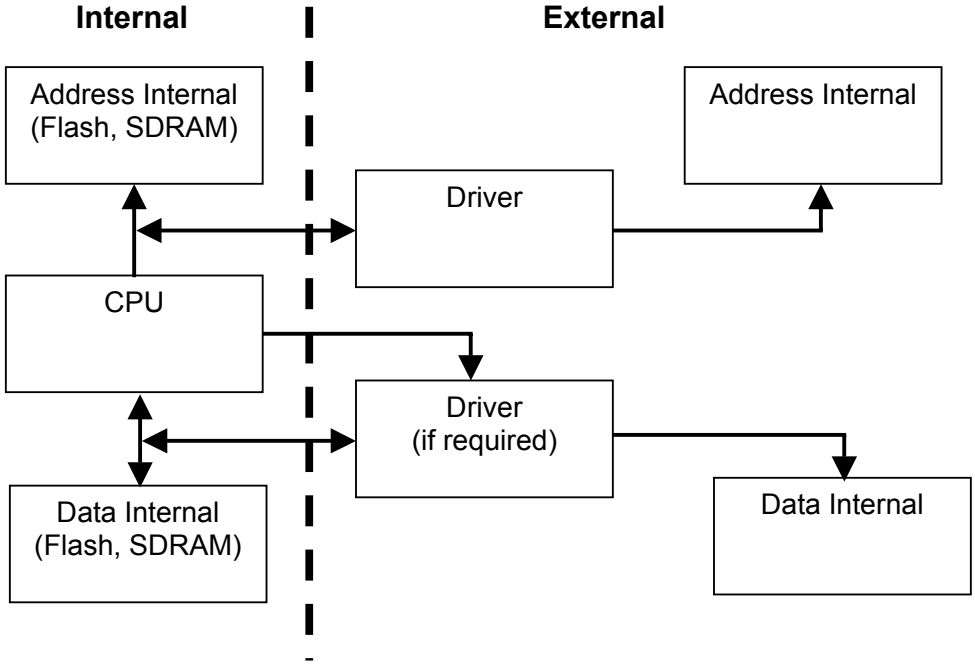


Illustration 3-5: Bus Structure

3.1.3.1 CPU Clock

The CPU clock is generated with an oscillator and multiplied, if required. The settings required for this are selected using the reset configuration word (refer to Specification MON8xx) without anything to be done in the hardware.

The tolerances include the output tolerance as also the frequency changes owing to temperature, variation of the supply voltage, ageing, shock and vibration.

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

CPU Clock Frequency [MHz]	Oscillator frequency [MHz]	Multiplication factor CPU	Division factor external bus	Clock frequency of external bus
50 ± 100 ppm	50 ± 100 ppm	1	1	50 ± 100 ppm
80 ± 100 ppm	16 ± 100 ppm	5	2	40 ± 100 ppm

Illustration 3-6: Clock frequencies

The central clock signal of the module is CLKOUT (= external bus clock). The total timing of the MPC860 is synchronous with this signal. It is also used to control the SDRAMs and is brought out on the wire strip. Since the signal is not buffered on the module itself, it must be handled with care and diligence on the baseboards, so that there are no repercussions on the module (SDRAMs):

- Very short lead lengths (max. 4 cm)
- Connect maximum one module
- A series resistance directly on the connector (typically. 33 Ω) can improve the signal quality

! note ! All these constraints can be overcome with the use of an external buffer. In order to maintain synchronism with CLKOUT, use of a zero-delay buffer is recommended (e.g. CY2305SC-1, Cypress).

3.1.3.2 RTC Pulse

The oscillator integrated in the CPU generates the RTC clock pulse of 32,768 kHz with the help of external quartz. This is used for the operation of the integrated RTC. During start-up of the MON8xx this is used as the reference clock pulse in order to determine the clock frequency of the CPU.

Tolerance of the RTC Pulse:

Nominal Frequency	Output Tolerance	Temperature coefficient. Max.	Ageing max.	Frequency change with shock max.
32,768 kHz	± 50 ppm	-0,04 ppm / °C^2	± 3 ppm / a	± 5 ppm

Illustration 3-7: Tolerance RTC-Pulse

! note ! With certain CPU variants and masks, an error of the CPU leads to a substantially increased consumption from VBAT, if the main supply is switched off. Please refer to the corresponding Errata sheets of Freescale.

©2004 by TQ-Components GmbH

3.1.3.3 CAN Pulse

The oscillator integrated in the first CAN controller generates a clock pulse of 16 MHz with the help of external quartz. The second controller derives its clock pulse from the CLKOUT of the first. This is to be taken into account while initializing the CAN controllers. The CAN controllers generate from their respective clock pulses the baud rates for the CAN bus.

Tolerance of the CAN Pulse:

Nominal frequency	Output tolerance	Temperature coefficient max.	Ageing max.
16 MHz	± 50 ppm	± 120 ppm	± 5 ppm / a

Illustration 3-8: Tolerance CAN Pulse

3.1.4. Reset Behavior

3.1.4.1 Reset Configuration

The system reads the reset configuration under normal circumstances from the bus (RSTCONF# = 0). However, if required, even the default configuration (RSTCONF# = 1 → Bits 0 .. 15 to 0) can be used, for which a high signal is given at RSTCONF#.

Bits	Name	Description	50 MHz	66 MHz	80 MHz
0	EARB	External arbitration. If this bit is set, external arbitration is assumed. If it is cleared, internal arbitration is performed.	0	0	0
1	IIP	Initial interrupt prefix. Defines the initial value of the MSR [IP], which defines the interrupt table location. If IIP is cleared (default), the MSR [IP] initial value is one; if it is set, the MSR [IP] initial value is zero.	1	1	1
2	BBE	Boot Burst Enable	0	0	0
		0 - The boot device does not support bursting.			
		1 - The boot device does support bursting.			

©2004 by TQ-Components GmbH

Bits	Name	Description	50 MHz	66 MHz	80 MHz
3	BDIS	Boot disable. If BDIS is set, memory bank 0 is invalid; i.e., BR0 [V] is cleared.	0	0	0
		0 - The memory controller is activated after reset so that it matches all addresses			
		1 - The memory controller is cleared after reset but is not activated.			
4–5	BPS	Boot port size. Defines the port size of the boot device as shown below:	00	00	00
		00 32-bit port size			
		01 8-bit port size			
		10 16-bit port size			
		11 Reserved			
6	–	Reserved for future use and should be allowed to float.	0	0	0
7–8	ISB	Initial internal space base select. Defines the initial value of the IMMR bits 0-15 and determines the base address of the internal memory space.	11	11	11
		00 0x00000000.			
		01 0x00F00000.			
		10 0xFF000000.			
		11 0xFFF00000.			
9–10	DBGC	Debug pin configuration. See 4.1 for details.	11	11	11
11–12	DPPC	Debug port pins configuration. See 4.1 for details.	01 / 00*	01 / 00*	01 / 00*

©2004 by TQ-Components GmbH

Bits	Name	Description	50 MHz	66 MHz	80 MHz
		See 4.1 for details.			
		Configuration for BDM-Debugging (JTAG/BDM# = 1 or open)			
		Configuration for JTAG-Test (JTAG/BDM# = 0)			
13–14	EBDF	External bus division factor. Defines the frequency division factor between GCLK1/GCLK2 and GCLK1_50/GCLK2_50. CLKOUT is similar to GCLK2_50. The system interface unit and memory controller use GCLK2_50 and GCLK1_50 to interface with the external system.	0	0	1
		00 Full speed bus			
		01 Half speed bus			
		10 Reserved			
		11 Reserved			
15	CLES	Core Little Endian Swap. Defines core access operation following reset.	0	0	0
		0 Big Endian			
		1 Little Endian			
* Depends on JTAG/BDM# signal					

Illustration 3-9: Reset Configuration

©2004 by TQ-Components GmbH

3.1.4.2 Reset Logic

Since it is critical to maintain the reset thresholds, components with low tolerances must be used accordingly, and a step for calibrating this must be incorporated in the module test.

- Voltage monitoring for 3,3 V (CPU, memory, other logic) matching with a fixed resistance, which, if required, is removed during test
- Voltage monitoring for 5 V (CAN controller)
- External Reset input
- Reset status displayed using LED (lights up, if SRESET# low)

The tolerances of the supply voltages and supervisory thresholds are displayed for each voltage in an appropriate diagram.

3.1.4.2.1 Tolerances and Reset Thresholds for VCC3V3

The tolerance for the external power supply (Pos. A, refer also to **Illustration 3-12:**):
VCC3V3 = 3,3 V –2,727 % / +5 % = 3,210 .. 3,465 V
The tolerance for the internal power supply/regulator (Pos. B, refer also to **Illustration 3-12:**):
VCC3V3 = 3,238 .. 3,446 V (standard temperature range, MAX651CSA)
VCC3V3 = 3,222 .. 3,463 V (extended temperature range, MAX651ESA)
The permissible operational range for the CPU and 3,3V logic (Pos. C, refer also to **Illustration 3-12:**):
VCC3V3 = 3,3 V ± 5 % = 3,135 .. 3,465 V
Tolerance of the supervisor circuit (standard temperature range, MAX816CSA):
U_{Reset}(matching resistance fitted) = 3,161 .. 3,287 V
U_{Reset} (matching resistance removed) = 3,079 .. 3,199 V
Tolerance of the supervisor circuit (extended temperature range, MAX816ESA):
U_{Reset}(matching resistance fitted) = 3,152 .. 3,296 V
U_{Reset}(matching resistance removed) = 3,070 .. 3,209 V

©2004 by TQ-Components GmbH

The matching resistance is removed, if the reset threshold measured lies over 3,210 V.

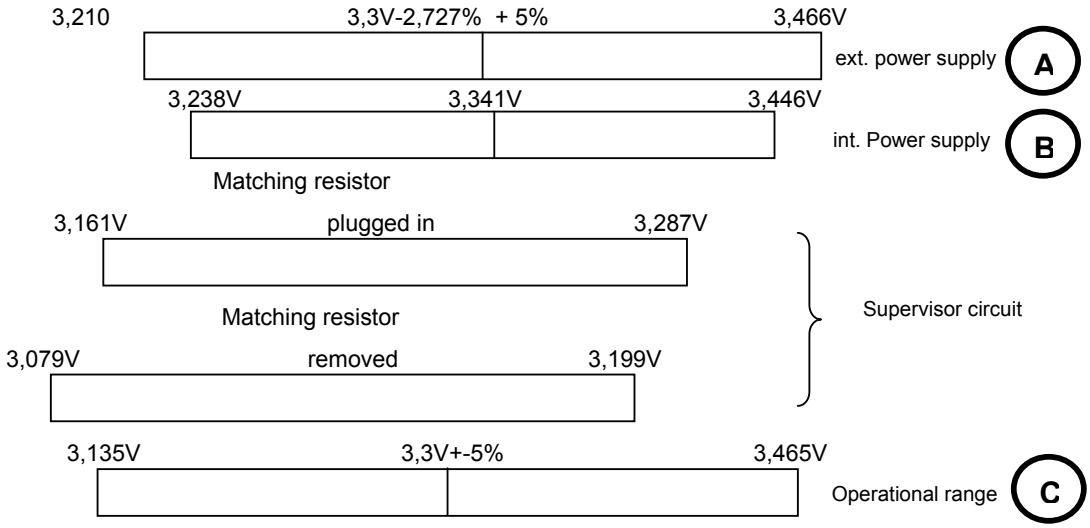


Illustration 3-10: Tolerances of 3,3V supply, standard temperature range

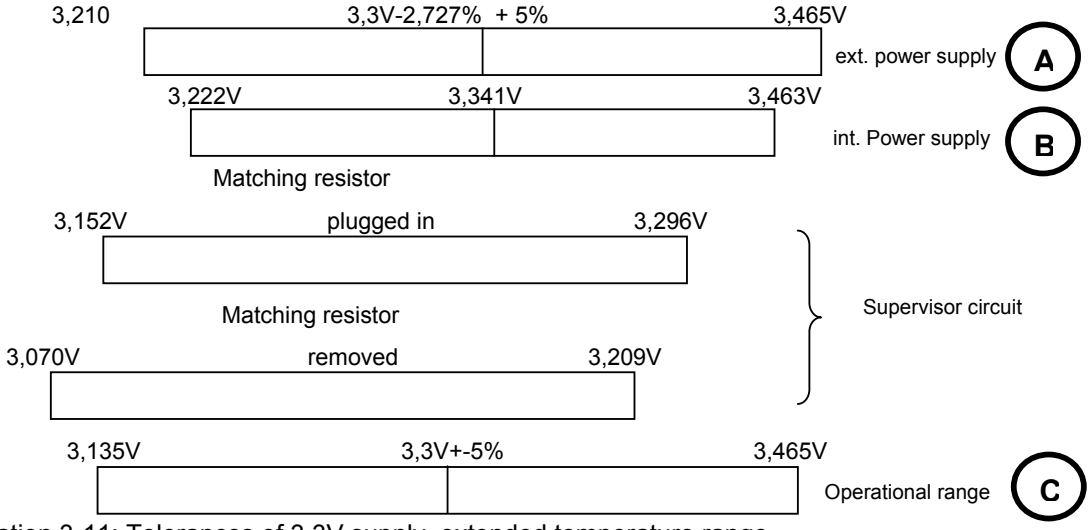


Illustration 3-11: Tolerances of 3,3V supply, extended temperature range

©2004 by TQ-Components GmbH

3.1.4.2.2 Tolerances and Reset Threshold for VCC5V

Tolerance of the power supply (Pos. D, refer also to **Illustration 3-12:**):

VCC5V = 5 V -4 % / +10 % = 4,8 .. 5,5 V

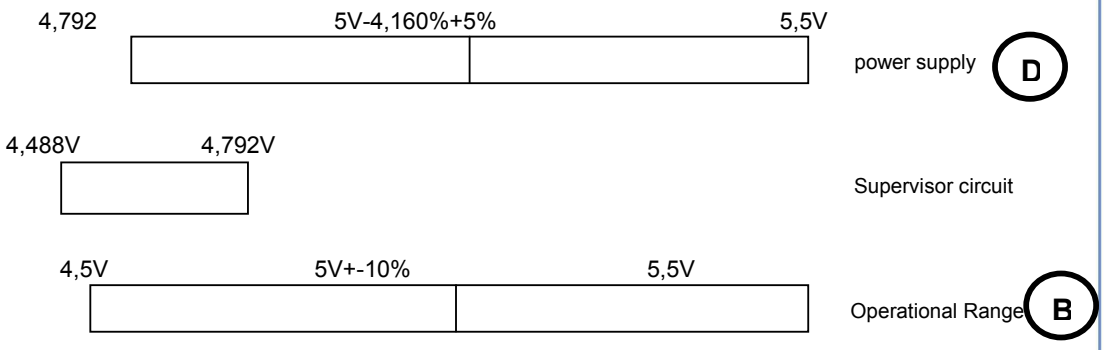
Tolerance of the supervisor circuit:

U_{Reset} = 4,638 V ± 3,27 % = 4,488 .. 4,792 V (MAX816CSA, MAX816ESA)

Permissible operational range of the CAN controller and 5V logic (Pos. E, refer also to **Illustration 3-12:**):

VCC5V = 5 V ± 10 % = 4,5 .. 5,5 V

The minimum value of the lower operational voltage limit appears tolerable. Matching is not necessary here.



3.1.4.2.3 External Reset Input

The RESIN# signal provides a debounced type, low active reset input. In order to prevent any backlash to the driver connected, this signal should be driven actively only to the ground (e.g. Open Collector/Open Drain output, push button towards ground or decoupling by means of a diode). For this the Low level of the signals MR# must be maintained as per the data sheet of the MAX816 **[9]**.

©2004 by TQ-Components GmbH

3.1.5. Power Supply (with different possibilities of the supply)

3.1.5.1 Possibilities of Power Supply

The power supply of the module is structured as follows:

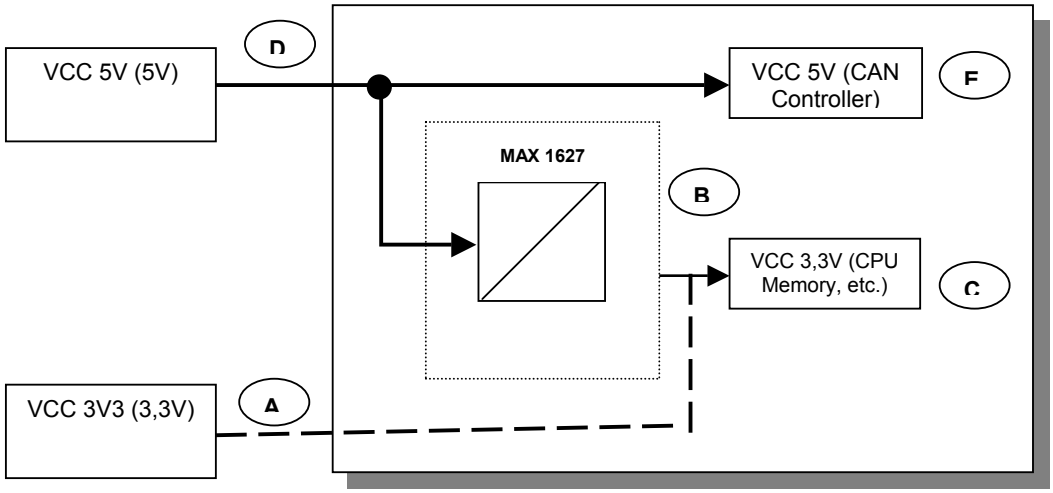


Illustration 3-12: Structure of the power supply

Depending on the module variant, the following possibilities are available for supplying power to the module:

- With CAN controller: Input voltage 5 V or 5 V and 3,3 V separate
- Without CAN controller: Input voltage 5 V or 3,3 V

With only a 5V supply one has to use a DC-DC converter from 5 V to 3,3 V.

3.1.5.2 3,3V Supply

Voltage VCC3V3 (external supply)	Ripple max.	Supply current max.	Output current regulator max.	Current capacity
3,210 .. 3,465 V	40 mV	548 mA	670 mA	–
Determined by the voltage range of the components and the supervisor threshold	Peak – Peak	Maximum value (worst case)	Guaranteed output current (worst case)	No consumption foreseen

Illustration 3-13: 3,3V Supply

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

3.1.5.2.1 Current Consumption at 3,3V

Component	Type	Current consumption@ 50 MHz max. [mA]	Current consumption @ 66 MHz max. [mA]	Current consumption @ 80 MHz max. [mA]
CPU	MPC860 [13]	231	265	275
FLASH	4 * 29LV160B (write) [3]	120	120	120
SDRAM	2 * MT48LC16M16A2TG-75 (160 mA, cont. burst, all banks active @ 100 MHz) [5]	160	211	128
RS232	MAX3222CAP (115 kBaud, 3 kW / 1000 pF), 2 * I_{typ} [8]	25	25	25
Watchdog	MAX816 [9]	@ 0	@ 0	@ 0
Gen. logic		@ 0	@ 0	@ 0
Total		536	621	548

Illustration 3-14: Current consumption at 3,3V

All values are valid in worst-case scenarios.

3.1.5.3 Regulator for 3,3 V

This option must be selected only if there is no external 3,3V power supply available for the module. A DC-DC converter generates the operational voltage of 3,3 V from the external power supply (5 V) for the CPU and all other 3,3 V modules.

- Current mode regulator with recovery diode
- Conversion 5 V → 3,3 V
- Design only for the module, no external loads permissible
- Iout(max) = 670 mA
- Variable Switching frequency 50 .. 120 kHz
- Low-ESR Tantalum

©2004 by TQ-Components GmbH

3.1.5.4 5V Power Supply

Voltage VCC5V (with CAN controller)	Voltage VCC5V (without CAN controller)	Ripple max.	Supply current max. (with regulator)	Supply current max. (without regulator)
4,792 .. 5,5 V	4,5 .. 5,5 V	60 mV	150 mA	602 mA
Determined by the voltage range of the components and the supervisor threshold	Determined by the design of the regulator	Peak - Peak	Maximum value (Worst Case)	Maximum value (Worst Case)

Illustration 3-15: 5V Supply

3.1.5.5 Current Consumption from 5 V Direct

Component	Type	Current consumption @ 50 MHz max. [mA]	Current consumption @ 66 MHz max. [mA]	Current consumption @ 80 MHz max. [mA]
CAN Controller	2 * AS82527 [6]	100	100	100
General Logic		@ 50	@ 50	@ 50
Total		150	150	150

Illustration 3-16: Current Consumption from 5V direct

TQM8xxL.HWM.0300.doc

©2004 by TQ-Components GmbH

3.1.5.6 Total Consumption at 5 V

If the module is supplied with 5 V power, then the total current drawn is the sum of that drawn directly from the 5 V supply, the input current of the DC-DC converter, which powers the 3,3 V logic:

Component	Type	Current consumption @ 50 MHz max. [mA]	Current consumption @ 66 MHz max. [mA]	Current consumption @ 80 MHz max. [mA]
5 V Logic	Refer to 3.2.3.1	150	150	150
Switching regulator	Input current	445	512	452
	= Consumption 3,3 V * (3,3 / 5) / eta (0,80)			
Total		595	662	602

Illustration 3-17 Total Consumption at 5V

3.1.5.7 Battery Buffering

The design includes buffering of the RTC integrated in the CPU.

VBAT Voltage	2,0 .. 3,6 V	
Current Drawn	10 µA...20 mA*	Maximum Value (Worst Case)

Illustration 3-18: Battery Buffering

! note !	This value is applicable to CPUs with the "RTC Bug", e.g. MPC860 up to and including C1 mask. Information about the current mask versions is given in the Errata sheets of Freescale.

©2004 by TQ-Components GmbH

3.1.6. Interfaces

3.1.6.1 Serial Interfaces

- Two internal UARTs
- Max. 115200 Baud
- Driver with RS232-compatible levels
- All signals available even without the driver
- Standard configuration Driver 2 * RxD / TxD

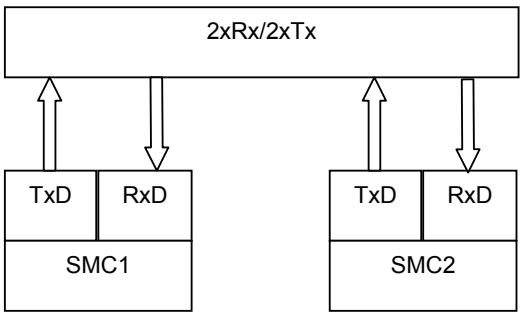


Illustration 3-19: Driver structure of the RS232 interfaces

3.1.6.2 Download Interface

- RxD and TxD
- Reset via the RS232 interface (RESIN#)
- Additional input lead of RS232 (ENMON#, can be read from the Port pin)

The Download Interface is an extension of the serial interface for control purposes. It consists of five signals, which are only available on the connector of the motherboard. On the starter kit STK8xxL they are combined with the connector for SMC1.

Pin*	Signal name	Type	Function
6	ENMON#	I	Switchover Monitor / normal boot procedure
3	SMTXD1	O	TxD of the debugging interface (SMC1, RS232 level)
5	GND	-	Ground
1	RESIN#	I	Reset input (Master reset of the reset module)
2	SMRXD1	I	RxD of the debugging interface (SMC1, RS232 level)
* on the starter kit STK8xxL			

Illustration 3-20: Signals of the download interface

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

The switchover signal ENMON# is implemented on the module by means of the port lead PA15 and a (discretely built) CMOS switch. This opens during the Reset phase, so that a high impedance coupling of the port lead with ENMON# becomes effective. After the reset phase the CMOS switch closes the port lead with low impedance with a time delay of about 10 ms. As a result of this, the CPU has sufficient time to evaluate the level of the reset phase.

3.1.6.3 BDM Interface

All leads of the Freescale BDM Interface (Debugging Interface) are brought out externally. As in the case of the TQS Download Interface the leads of the BDM Interface are brought out exclusively to the connector of the motherboard. It consist as of the following signals:

Pin*	Signal name	Type	Function
1	FRZ# (VFSL0)**	O	Freeze (CPU history buffer status)
2	SRESET#	I/O	Soft reset
3	DGND	-	Ground
4	DSCK/TCK	I	Clock
5	DGND	-	Ground
6	FRZ# (VFLS1)**	0	Freeze (CPU history buffer status)
7	HRESET#	I/O	Hard reset
8	DSDI/TDI	I	Data input
9	VCC3V3	-	Power Supply
10	DSDO/TDO	O	Data output
*	on the Starter kit STK8xxL		
**	alternative assignment in brackets		

Illustration 3-21: Signals of the BDM interface

©2004 by TQ-Components GmbH

3.1.7. Module connector

3.1.7.1 Pin Assignment

- 32 Bit data bus
- 32 Bit address bus
- All port I/O pins

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
Address Bus					
A0	B19	I/O, TS	Address A0 (MSB)	50	X1-111
A1	B18	I/O, TS	Address A1	50	X1-110
A2	A18	I/O, TS	Address A2	50	X1-109
A3	C16	I/O, TS	Address A3	50	X1-108
A4	B17	I/O, TS	Address A4	50	X1-107
A5	A17	I/O, TS	Address A5	50	X1-106
A6	B16	I/O, TS	Address A6	40	X1-105
A7	A16	I/O, TS	Address A7	40	X1-104
A8	D15	I/O, TS	Address A8	10	X1-103
A9	C15	I/O, TS	Address A9	10	X1-102
A10	B15	I/O, TS	Address A10	10	X1-101
A11	A15	I/O, TS	Address A11	20	X1-100
A12	C14	I/O, TS	Address A12	20	X1-99
A13	B14	I/O, TS	Address A13	20	X1-98
A14	A14	I/O, TS	Address A14	20	X1-97
A15	D12	I/O, TS	Address A15	20	X1-96
A16	C13	I/O, TS	Address A16	20	X1-95
A17	B13	I/O, TS	Address A17	20	X1-94
A18	D9	I/O, TS	Address A18	10	X1-93
A19	D11	I/O, TS	Address A19	20	X1-92
A20	C12	I/O, TS	Address A20	10	X1-91
A21	B12	I/O, TS	Address A21	10	X1-90
A22	B10	I/O, TS	Address A22	≈ 5	X1-89
A23	B11	I/O, TS	Address A23	≈ 5	X1-88
A24	C11	I/O, TS	Address A24	5	X1-87
A25	D10	I/O, TS	Address A25	5	X1-86
A26	C10	I/O, TS	Address A26	5	X1-85
A27	A13	I/O, TS	Address A27	5	X1-84
A28	A10	I/O, TS	Address A28	5	X1-83
A29	A12	I/O, TS	Address A29	5	X1-82
A30	A11	I/O, TS	Address A30	45	X1-81

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
A31	A9	I/O, TS	Address A31 (LSB)	45	X1-80

Data Bus

D0	W14	I/O, TS	Data D0 (MSB)	9	X2-88
D1	W12	I/O, TS	Data D1	≈ 5	X2-89
D2	W11	I/O, TS	Data D2	9	X2-90
D3	W10	I/O, TS	Data D3	9	X2-91
D4	W13	I/O, TS	Data D4	9	X2-92
D5	W9	I/O, TS	Data D5	9	X2-93
D6	W7	I/O, TS	Data D6	9	X2-94
D7	W6	I/O, TS	Data D7	≈ 5	X2-95
D8	U13	I/O, TS	Data D8	25	X2-96
D9	T11	I/O, TS	Data D9	25	X2-97
D10	V11	I/O, TS	Data D10	25	X2-98
D11	U11	I/O, TS	Data D11	30	X2-99
D12	T13	I/O, TS	Data D12	25	X2-100
D13	V13	I/O, TS	Data D13	30	X2-101
D14	V10	I/O, TS	Data D14	25	X2-102
D15	T10	I/O, TS	Data D15	30	X2-103
D16	U10	I/O, TS	Data D16	30	X2-104
D17	T12	I/O, TS	Data D17	30	X2-105
D18	V9	I/O, TS	Data D18	30	X2-106
D19	U9	I/O, TS	Data D19	30	X2-107
D20	V8	I/O, TS	Data D20	30	X2-108
D21	U8	I/O, TS	Data D21	30	X2-109
D22	T9	I/O, TS	Data D22	30	X2-110
D23	U12	I/O, TS	Data D23	30	X2-111
D24	V7	I/O, TS	Data D24	30	X2-112
D25	T8	I/O, TS	Data D25	30	X2-113
D26	U7	I/O, TS	Data D26	30	X2-114
D27	V12	I/O, TS	Data D27	30	X2-115
D28	V6	I/O, TS	Data D28	30	X2-116
D29	W5	I/O, TS	Data D29	30	X2-117
D30	U6	I/O, TS	Data D30	30	X2-118
D31	T7	I/O, TS	Data D31 (LSB)	30	X2-119

Bus Control

IRQ0#	V14	I	Interrupt Request 0 (NMI), Pull-Up 4k7	50	X1-2
IRQ1#	U14	I	Interrupt Request 1, Pull-Up 4k7	50	X1-3
IRQ2#/RS	H3	I/O; TS	Interrupt Request 2 /	50	X1-4

©2004 by TQ-Components GmbH

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
V#			Reservation, Pull-Up 4k7		
IRQ3#	V3	I	Interrupt Request 3, Pull-Up 4k7	50	X1-5
IRQ_CAN# / IRQ4#	V5	I	Interrupt Request 4, used for CAN Interrupt, connected to P2.6/INT# of both AS82527 devices, Pull-Up 4k7	35	X1-6
IRQ5#	W4	I	Interrupt Request 5, Pull-Up 4k7	50	X1-7
IRQ6#	V4	I	Interrupt Request 6, Pull-Up 4k7	50	X1-8
IRQ7#	W15	I	Interrupt Request 7, Pull-Up 4k7	50	X1-9
RD/WR#	B2	I/O, TS	Read / Write	50	X2-73
BB#	E1	I/O, TS	Bus Busy, Pull-Up 2k2	50	X2-75
BG#	E2	I/O	Bus Grant	50	X2-74
BR#	G4	I/O	Bus Request, Pull-Up 4k7	50	X2-76
BURST#	F1	I/O, TS	Burst Transaction	50	X2-82
BDIP#/GPL_B5#	D2	I/O, TS	Burst Data In Progress / General Purpose Line B5	50	X1-63
BI#	E3	I/O, TS	Burst Inhibit, Pull-Up 4k7	50	X2-81
TS#	F3	I/O, TS	Transfer Start, Pull-Up 4k7	50	X2-83
TA#	C2	I/O, TS	Transfer Acknowledge, Pull-Up 2k2	50	X2-77
TEA#	D1	I/O, OD	Transfer Error Acknowledge, Pull-Up 2k2	50	X2-80
TSIZ0/REG#	B9	I/O, TS	Transfer Size 0 / Register	50	X2-78
TSIZ1	C9	I/O, TS	Transfer Size 1	50	X2-79
IRQ4#/KR#/ RETRY#	K1	I/O, TS	Interrupt Request 4 / Kill Reservation / Retry, Pull-Up 4k7	50	X2-72
CR#/IRQ3#	F2	I	Cancel Reservation / Interrupt Request 3	50	X2-70

Memory Controller

BS_A0#	D8	O	Byte Select A0	45	X1-56
BS_A1#	C8	O	Byte Select A1	45	X1-57
BS_A2#	A7	O	Byte Select A2	45	X1-58
BS_A3#	B8	O	Byte Select A3	45	X1-59

©2004 by TQ-Components GmbH

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
WE0#/BS_B0#	C7	O	Byte Select A0 / Write Enable 0	50	X1-76
WE1#/BS_B1#	A6	O	Byte Select A1 / Write Enable 1	50	X1-77
WE2#/BS_B2#	B6	O	Byte Select A2 / Write Enable 2	50	X1-78
WE3#/BS_B3#	A5	O	Byte Select A3 / Write Enable 3	50	X1-79
CS_FLASH0#/ CS0#	C3	O	Chip Select 0 (Flash, Boot Chip Select)	35	X1-71
CS_FLASH1#/ CS1#	A2	O	Chip Select 1 (Flash)	35	X1-70
CS_SDRAM0#/ CS2#	D4	O	Chip Select 2 (SDRAM)	40	X1-69
CS_CAN#/ CS3#	E4	O	Chip Select 3 (CAN)	40	X1-68
CS4#	A4	O	Chip Select 4	50	X1-67
CS5#	B4	O	Chip Select 5	50	X1-66
CS6#/CE1_B#	D5	O	Chip Select 6 / Card Enable 1 Slot B	50	X1-65
CS7#/CE2_B#	C4	O	Chip Select 7 / Card Enable 2 Slot B	50	X1-64
CE1_A#	B3	O	Card Enable 1 Slot A	50	X1-54
CE2_A#	A3	O	Card Enable 2 Slot A	50	X1-55
OE#/GPL_AB1#	C6	O	Output Enable / General Purpose Line A1 / B1, used for SDRAM and FLASH	10	X1-73
GPL_AB2#	B5	O	General Purpose Line A2 / B2, used for SDRAM and CAN	30	X1-74
GPL_AB3#	C5	O	General Purpose Line A3 / B3, used for SDRAM	40	X1-75
GPL_AB0#	D7	O	General Purpose Line A0 / B0	40	X1-72
UPWAITA/ GPL_A4#	C1	I/O	UPM Wait A / General Purpose Line A4, used for CAN	50	X1-60
UPWAITB/ GPL_B4#	B1	I/O	UPM Wait B / General Purpose Line B4	30	X1-61

©2004 by TQ-Components GmbH

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
GPL_A5#	D3	O	General Purpose Line A5, used for CAN	45	X1-62
AS#	L3	I	Address Strobe, Pull-Up 4k7	50	X2-69
BADDR28	M3	O	Burst Address 28	50	X2-68
BADDR29	M2	O	Burst Address 29	50	X2-67
BADDR30/ REG#	K4	O	Burst Address 30 / Register	50	X2-66

PCMCIA

WAIT_A#	R3	I	Wait Slot A, Pull-Up 4k7	50	X1-10
ALE_A	K2	O	Address Latch Enable A, Pull-Up 4k7	50	X1-11
IP_A0	T5	I	Input Port A0, Pull-Up 4k7	50	X1-12
IP_A1	T4	I	Input Port A1, Pull-Up 4k7	50	X1-13
IP_A2	U3	I	Input Port A2, Pull-Up 4k7	50	X1-14
IP_A3	W2	I	Input Port A3, Pull-Up 4k7	50	X1-15
IP_A4	U4	I	Input Port A4, Pull-Up 4k7	50	X1-16
IP_A5	U5	I	Input Port A5, Pull-Up 4k7	50	X1-17
IP_A6	T6	I	Input Port A6, Pull-Up 4k7	50	X1-18
IP_A7	T3	I	Input Port A7, Pull-Up 4k7	50	X1-19
WAIT_B#	R4	I	Wait Slot B, Pull-Up 4k7	50	X1-24
ALE_B	J1	O	Address Latch Enable B, Pull-Up 4k7	50	X1-25
IP_B0/VFLS0	H2	I	Input Port B0 / CPU history buffer status 0, Pull-Up 4k7	50	X1-33
IP_B1/VFLS1	J3	I	Input Port B1 / CPU history buffer status 1, Pull-Up 4k7	50	X1-32
IP_B2	J2	I	Input Port B2, Pull-Up 4k7	50	X1-31
IP_B3	G1	I	Input Port B3, Pull-Up 4k7	50	X1-30
IP_B4	G2	I	Input Port B4, Pull-Up 4k7	50	X1-29
IP_B5	J4	I	Input Port B5, Pull-Up 4k7	50	X1-28
IP_B6	K3	I	Input Port B6, Pull-Up 4k7	50	X1-27
IP_B7	H1	I	Input Port B7, Pull-Up 4k7	50	X1-26
OP0	L4	O	Output Port 0	50	X1-21
OP1	L2	O	Output Port 1	50	X1-20
OP2/MODCK1	L1	I/O	Output Port 2 / Mode Clock 1	45	X1-22
OP3/MODCK2	M4	I/O	Output Port 3 / Mode Clock 2	45	X1-23

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin

Other CPU Signals

SPARE1/ MII_CRS	B7	I	MII Carrier Receive Sense / Spare 1	50	X2-87
SPARE2/ MII_MDIO	H18	I/O	MII Management Data / Spare 2	50	X2-86
SPARE3/ MII_TX_EN	V15	O	MII Transmit Enable / Spare 3	50	X2-85
SPARE4/ MII_COL	H4	I	MII Collision / Spare 4	50	X2-84
CLKOUT	W3	O	Clock Out	30	X1-40
EXTCLK	N2	I	External Clock	50	X1-39
TEXP	N3	O	Timer Expired	50	X1-36
PORESET#	R2	O	Power-On Reset, connected to Voltage Supervisor output (3,3 and 5 V)	50	X1-35
HRESET#	N4	I/O, OD	Hard Reset, Pull-Up 1k	50	X1-37
SRESET#	P2	I/O, OD	Soft Reset, Pull-Up 10 k, LED with 220 Ω to VCC3V3	50	X1-42
RSTCONF#	P3	I	Reset Configuration, Pull-Down 1 k	50	X1-38
DSDI/TDI	H17	I	Development Serial Data In / Test Data In	50	X2-44
DSDO/TDO	G17	O	Development Serial Data Out / Test Data Out	50	X2-45
DSCK/TCK	H16	I	Development Serial Clock / Test Clock, Pull-Down 1 k	50	X2-46
TMS	G18	I	Test Mode Select, Pull-Up 10 k	50	X2-47
FRZ/IRQ6#	G3	I/O	Freeze / Interrupt Request 6, Pull-Up 4k7	50	X2-71

Port A

PA0	U19	I/O	Port A0	50	X2-28
PA1	T19	I/O	Port A1	50	X2-29
PA2	R18	I/O	Port A2	50	X2-30
PA3	P17	I/O	Port A3	50	X2-31
PA4	P19	I/O	Port A4	50	X2-32
PA5	N18	I/O	Port A5	50	X2-33
PA6	M17	I/O	Port A6	50	X2-34
PA7	M19	I/O	Port A7	50	X2-35

©2004 by TQ-Components GmbH

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
PA8	L17	I/O	Port A8	50	X2-36
PA9	K18	I/O	Port A9	50	X2-37
PA10	J17	I/O	Port A10	50	X2-38
PA11	G16	I/O	Port A11	50	X2-39
PA12	F17	I/O	Port A12	50	X2-40
PA13	E17	I/O	Port A13	50	X2-41
PA14	D17	I/O	Port A14	50	X2-42
PA15	C18	I/O	Port A15 (via analog switch)	≈ 10	X2-43

Port B

PB14	U18	I/O	Port B14	50	X2-48
PB15	R17	I/O	Port B15	50	X2-49
PB16	N16	I/O	Port B16	50	X2-50
PB17	P18	I/O	Port B17	50	X2-51
PB18	N17	I/O	Port B18	50	X2-52
PB19	N19	I/O	Port B19	50	X2-53
PB20/SMRXD2#	L16	I/O	Port B20, used as SMRXD2#, connected to RS232-Driver TTL-Output via 4k7 resistor to allow other usage	50	X2-54
PB21/SMTXD2#	K16	I/O	Port B21, used as SMTXD2#, connected to RS232-Driver TTL-Input	50	X2-55
PB22	L19	I/O	Port B22	50	X2-56
PB23	K17	I/O	Port B23	50	X2-57
PB24/SMRXD1# RXD3#	J18	I/O	Port B24, used as SMRXD1# or RXD3#, connected to RS232-Driver TTL-Output via 4k7 resistor to allow other usage	50	X2-58
PB25/SMTXD1#/ TXD3#	J16	I/O	Port B25, used as SMTXD1# or TXD3#, connected to RS232-Driver TTL-Input	50	X2-59
PB26	F19	I/O	Port B26	50	X2-60
PB27	E19	I/O	Port B27	50	X2-61
PB28	D19	I/O	Port B28	50	X2-62
PB29	E16	I/O	Port B29	50	X2-63
PB30	C19	I/O	Port B30	50	X2-64
PB31	C17	I/O	Port B31	50	X2-65

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
Port C					
PC4	T17	I/O	Port C4	50	X2-16
PC5	T18	I/O	Port C5	50	X2-17
PC6	R19	I/O	Port C6	50	X2-18
PC7	M16	I/O	Port C7	50	X2-19
PC8	M18	I/O	Port C8	50	X2-20
PC9	L18	I/O	Port C9	50	X2-21
PC10	K19	I/O	Port C10	50	X2-22
PC11	J19	I/O	Port C11	50	X2-23
PC12	F18	I/O	Port C12	50	X2-24
PC13	E18	I/O	Port C13	50	X2-25
PC14	D18	I/O	Port C14	50	X2-26
PC15	D18	I/O	Port C15	50	X2-27
Port D					
PD3	W16	I/O	Port D3	50	X2-3
PD4	U16	I/O	Port D4	50	X2-4
PD5	U15	I/O	Port D5	50	X2-5
PD6	V16	I/O	Port D6	50	X2-6
PD7	T15	I/O	Port D7	50	X2-7
PD8	W17	I/O	Port D8	50	X2-8
PD9	V17	I/O	Port D9	50	X2-9
PD10	W18	I/O	Port D10	50	X2-10
PD11	T16	I/O	Port D11	50	X2-11
PD12	R16	I/O	Port D12	50	X2-12
PD13	V18	I/O	Port D13	50	X2-13
PD14	V19	I/O	Port D14	50	X2-14
PD15	U17	I/O	Port D15	50	X2-15

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
Non-CPU Signals					
RESIN#	1	I	Reset Input (Master Reset Input of Voltage Supervisor), Pull-Up 4k7	–	X1-34
HRESETF#	1	I	Flash Reset Signal (12 V may be applied without damaging the module – however, this is not recommended)	–	X1-44

©2004 by TQ-Components GmbH

Signal	No. of Pins	Type	Description	Ext. Load Cap. max. [pF]	Module Pin
ENMON#	1	I	Monitor Enable (enables MON8xx interactive Mode), Pull-Up 10 k	–	X1-41
CKE	1	I	SDRAM Clock Enable, Pull-Up 4k7	–	X1-45
JTAG/BDM #	1	I	JTAG / BDM Configuration (via Hard Reset Configuration), Pull-Up 10 k	–	X1-43
SMRXD1	1	I	SMC1 Receive Data, RS232 level	–	X1-52
SMTXD1	1	O	SMC1 Transmit Data, RS232 level	1000 || 3 kΩ	X1-53
SMRXD2	1	I	SMC2 Receive Data, RS232 level	–	X1-50
SMTXD2	1	O	SMC2 Transmit Data, RS232 level	1000 || 3 kΩ	X1-51
RX0_CAN1	1	I	CAN controller 1 RX0	–	X1-49
TX0_CAN1	1	O	CAN controller 1 TX0	50	X1-48
RX0_CAN2	1	I	CAN controller 2 RX0	–	X1-47
TX0_CAN2	1	O	CAN controller 2 TX0	50	X1-46

Power Supply

VCC5V	3	V	5 V Supply (CAN Controller, DC/DC converter input)	–	X1-116 X1-118 X1-120
VCC3V3	3	V	3,3 V Supply (DC/DC converter output)	–	X1-112 X1-113 X1-114
VBAT	1	V	Battery Voltage, connected via Schottky Diode and RC combination (1 k / 100 n) to KAPWR	–	X2-1
DGND	6	V	(Digital) Ground	–	X1-1 X1-115 X1-117 X1-119 X2-2 X2-120

Illustration 3-22: Pin assignment

For connection of the power supply refer to 3.1.5.1

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

3.2 Mechanical Specification

3.2.1. General Information

- Two-rowed, high pole SMD connector with grid of 0,8 mm 2 * 120-pole
- The combination with different matching connectors facilitates different board heights, in order to offer adaptibility to the assembly on the main board
- Double-sided SMD assembly
- Multilayer PCB in Micro-Via technique

3.2.2. Dimensions

- PCB dimensions 54 mm * 44 mm
- PCB Height: a + b + c = 10,6 mm
- Free height under the module: a - d = 2,6 mm

The shaded areas in the following figure refer to blocked areas, which should be kept free in the motherboard for the extraction tool MOZI8xxL. The blocked areas are symmetric. The positions shown are those in plugged-in condition (right) and during plug-in (left).

©2004 by TQ-Components GmbH

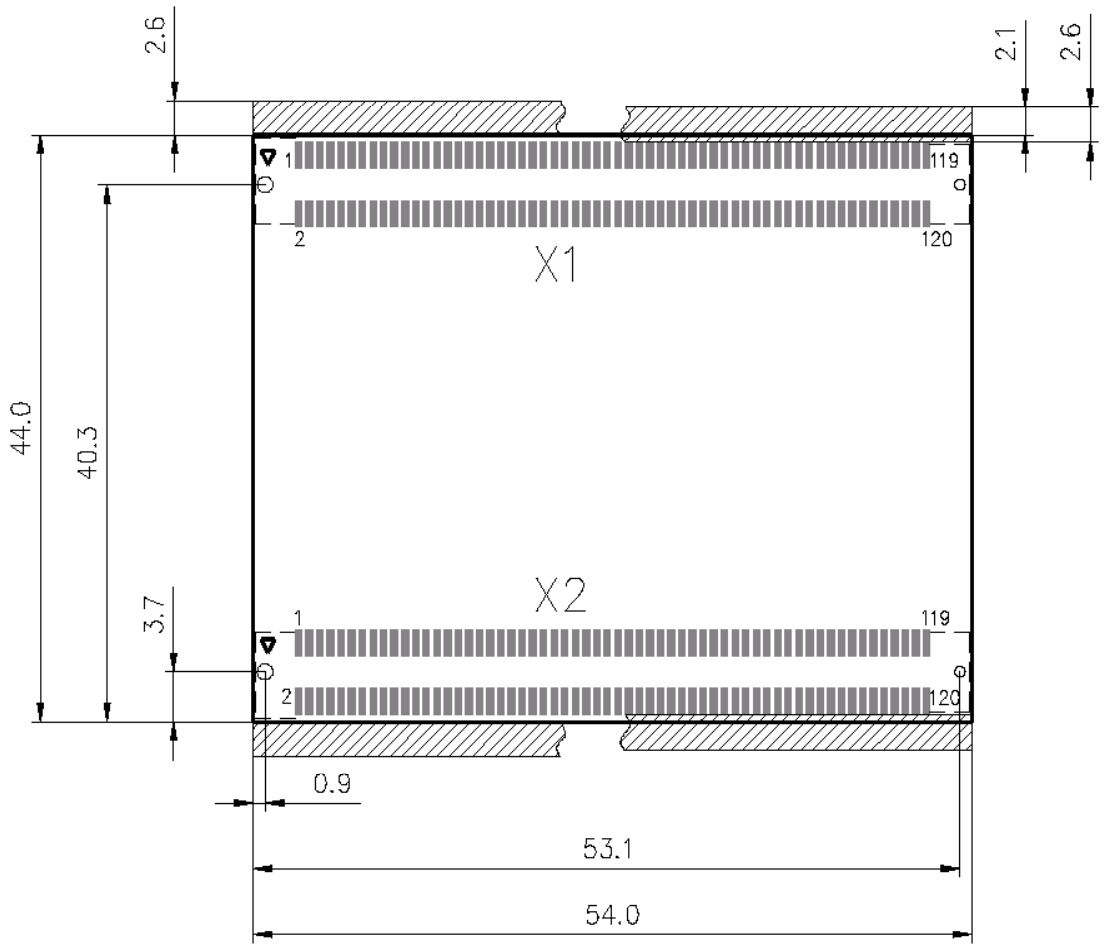


Illustration 3-23 Top view of the PCB

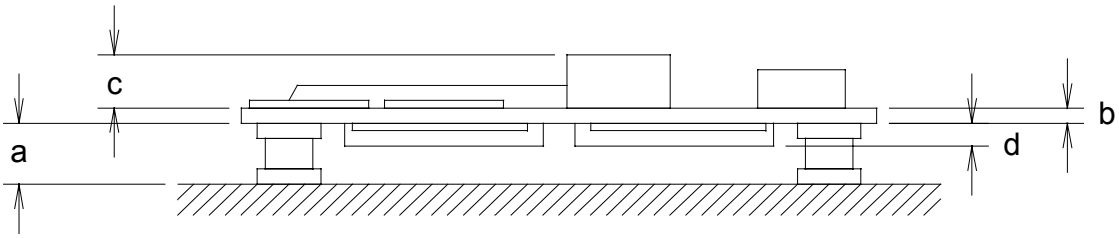


Illustration 3-24: PCB heights (not to scale)

Dimension	Value [mm]	Remarks
a	5,0 ± 0,2	Combination of module connector with counter-part; with other connectors on the motherboard even 6, 7 and 8 mm are possible
b	1,5 ± 0,15	Printed Circuit Board
c	3,5 ± 0,5	Memory choke [10] (maximum height on the top side)
d	2,35 max.	CAN controller [7] (maximum height on the bottom side)

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

3.2.3. Connector

Board-to-Board Distance	Module				Base Board Connector		
	No. of Pins	Qty.	Supplier	Order No.	No. of Pins	Supplier	Order No.
5 mm	120	2	AMP /Berg	177983-5 /61082-121000	120	AMP / Berg	177984-5/ 61083-121000
6 mm					120	AMP / Berg	5-179029-5/ 61083-122000
7 mm					120	AMP / Berg	5-179030-5/ 61083-123000
8 mm					120	AMP / Berg	5-179031-5/ 61083-124000

Illustration 3-25: Overview of Connector

3.2.4. Tips on handling

	To ensure elegant removal (plug-out) of the module from the motherboard making use of the extraction tool MOZI8xxL, which is supplied along with the starter kit, is mandatory.

©2004 by TQ-Components GmbH

4 Variant codes

TQM a1 L v w x y z - a2 b t

t: Temperaturbereich
blank = 0°C..70°C
I = -40°C..+85°C

b: CPU-Clock
50 = 50MHz
66 = 66MHz
80 = 80MHz

a2: Microprozessor Derivat

DE = DEZP
P = PZP
SR = SRZP
T = TZP

z: Optionale Bestückung
0 = ohne Optionen
1 = mit Schaltregler
2 = mit RS232 Treiber

y: Steckerbauhöhe
A = 5mm

x: CAN Ausstattung
0 = ohne CAN Ausstattung
1 = 1. Controller bestückt
2 = 1. und 2. Controller bestückt

w: SDRAM Ausstattung
B = 16MByte
C = 32MByte
D = 64MByte
E = 128MByte

v: Flash Ausstattung
C = 4MByte
D = 8MByte

a1: Mikroprozessor Version
823 = XPC823
850 = XPC850
855 = XPC855
860 = XPC860
862 = XPC862

Illustration 4-1: Variant Codes

©2004 by TQ-Components GmbH

The following types are available ex-stock:

TQM855L-AA	TQM855LDB0A3-T80	- XPC855TZP80 - 8MB Flash - 16MB SDRAM - kein CAN - mit Schaltregler - mit RS232 Treiber - 80MHz Takt - Temperaturbereich 0°C...70°C
TQM855L-AB	TQM855LDB0A3-T50	- XPC855TZP50 - 8MB Flash - 16MB SDRAM - kein CAN - mit Schaltregler - mit RS232 Treiber - 50MHz Takt - Temperaturbereich 0°C...70°C
TQM860L-AA	TQM860LDB0A3-P80	- XPC860PZP80 - 8MB Flash - 16MB SDRAM - kein CAN - mit Schaltregler - mit RS232 Treiber - 80MHz Takt - Temperaturbereich 0°C...70°C
TQM860L-AB	TQM860LDB0A3-P50	- XPC860PZP50 - 8MB Flash - 16MB SDRAM - kein CAN - mit Schaltregler - mit RS232 Treiber - 50MHz Takt - Temperaturbereich 0°C...70°C
TQM860L-AD	TQM860LDDBA3-P50	- XPC860PZP50 - 8MB Flash - 64MB SDRAM - CAN Controller 1 und 2 bestückt - mit Schaltregler - mit RS232 Treiber - 50MHz Takt - Temperaturbereich 0°C...70°C
TQM862L-AA	TQM862LDB0A3-SR80	- XPC860SRZP80 - 8MB Flash - 16MB SDRAM - kein CAN - mit Schaltregler - mit RS232 Treiber - 80MHz Takt - Temperaturbereich 0°C...70°C

Illustration 4-2: Standard Types of Modules

©2004 by TQ-Components GmbH

5 Environmental Conditions

5.1 Climatic Conditions and Areas of Application

- Ambient temperature : 0 .. 70 °C, optional -40°C .. +85°C
- Storage temperature: -20 .. + 100 °C
- Protection type : IP00 (no protection against dust and moisture)

5.2 Installation Instructions

The critical component with respect to heating is the CPU. In open-air condition (natural convection possible) operation is possible over the complete ambient temperature range without any special cooling measures. When mounting the module in a cabinet, the following must be taken care of:

- Within a closed cabinet, in general, there would be temperature rise. What is important for the operational safety is the temperature in the vicinity of the module, so that the maximum permissible temperature for the complete cabinet is reduced. This can be improved e.g. by direct thermal connection of the module (heat-conducting sponge / rubber) to a heat sink, or by forced cooling.
- Within the closed cabinet the module could also get heated by other sources of heat. The remedy for this is as given above, or by isolation of the heat source(s).

5.3 Reliability and Life-span

For the module a FIT-Rate of 800 * 10-9 / h has been calculated [12].
For the connectors used a minimum of 100 connection cycles has been guaranteed [11].

5.4 Product Qualification

With respect to product qualification the PCBs have been tested as per the following standards, or the tests are in progress:

5.4.1. Mechanical Environmental Influences

Vibration	EN60068-2-6
Shock	EN60068-2-27

©2004 by TQ-Components GmbH

5.4.2. Temperature Tests

Temperature change	EN60068-2-14
Cold storage	EN60068-2-1
Warm storage	EN60068-2-2
Storage under moist conditions	DIN IEC 68-2-3

5.4.3. EMI/EMC

Basic technical standard Interference emission,
Part 1: Living quarters, business and industrial areas
as also small enterprises EN50081

5.4.4. EMC Passive / Radiation

Basic technical standard Interference susceptibility,
Part 2: Industrial area EN50082

5.4.5. ESD

Basic technical standard Interference susceptibility,
Part 2: Industrial area EN50082

5.4.6. UL Approval

A UL certification can be obtained if requried.

6 Safety requirements and Personnel Protection

6.1 EMI/EMC Requirements

The conformance to the standards is fulfilled by using a reference design. The starter kit STK8xxL with the corresponding external circuit is used as a reference design.
The module has been developed diligently and painstakingly to ensure conformance to electromagnetic interference / compatibility (EMI/EMC) requirements. In spite of this, depending on the target system, certain radio interference suppression measures may be necessary to ensure that specific limit values are not violated for the complete system.

©2004 by TQ-Components GmbH

The following measures are recommended:

- Robust grounding measures (sufficient ground surface) on the PCB
- With metal cabinets a good (minimum with respect to HF) connection of the PCB ground to the cabinet potential
- Sufficient blocking condensors at all supply voltages
- Leads carrying high frequency or continuous pulses (e.g. Clock) should be of short length; avoid stray pick-up in other signals by maintaining a distance and / or appropriate shielding
- Filtering of all signals which can be connected externally (even "slow" and DC voltage signals can radiate HF indirectly)

6.2 ESD Requirements

It is meaningful to provide a good protection against electrostatic discharge directly at the inputs of a system, so that there is no coupling in the path from the input to the protective circuit in the system. Since these measures always have to be implemented on the motherboard, no special protective measures have been incorporated in the module itself. The modules used offer a certain degree of protection as per the specification, which, however, in general, is not adequate to comply with statutory requirements without additional measures

The following measures are recommended:

- Generally applicable: Shielding of the leads/wires (shielding on both sides connected firmly with ground / body of the cabinet)
- For power supply: Protection using supressor diode(s)
- Slow signal leads/wires: RC filtering, possibly Zener diode

Fast signal leads/wires: Integrated protection modules (suppressor diode arrays)

6.3 Operational Safety and Personnel Protection

A special test has not been performed owing to the voltages encountered (≤ 5 V DC).

©2004 by TQ-Components GmbH

7 Annexure

7.1 Software Support

7.1.1. Monitor Software

The monitor program MON8xx is the standard basic software delivered on TQM8xxL modules. After connecting a serial interface and the power supply the monitor program enables communication with the module with the help of a starter kit STK8xxL. The MON8xx offers basic functions for commissioning the TQM8xxL. These are divided into the following areas:

- Monitor functions:

Memory and register monitor to address the memory and the register of the MPC8xx, extension possibilities to address further - also external – memory-mapped I/Os. It also offers simple I/O functions such as memory editing, dump, change register, as also the possibility, to load S-Record-Files in RAM or Flash.

- Automatic Application start:

After a reset either the monitor or an application / an operating system can be started. For this purpose, the MON8xx reads the port pin provided on the debugging interface (Signal ENMON#), and passes control either to the monitor, or starts an application or an operating system.

The specification and functionality of the MON8xx is described in a special document.

©2004 by TQ-Components GmbH

7.1.2. Configuration of the SDRAMs

The SDRAMs are controlled by the UPMA. The UPM is programmed for SDRAM operation with single and burst read and write, CAS Latency 2, sequential operation (no interleave) and 4xburst. The allocation of the sequencer table of the UPMA, all other configurations for the operation of SDRAMs are illustrated in the following .CMM file. This can be executed directly with a Lauterbach debugger, for other development environments, the syntax must be adapted accordingly.
The initialization differs from that done by the monitor MON8xx in the following manner:

- Initialization for 8 column SDRAMs (16 and 64 MBit) implemented → SDRAMs with 9 columns (128 and 256 MBit) are only half used.
- Refresh rate is permanently set to the maximum possible value

```
; ------------------------------------------------------------
------------
; Memory Mapping
; ------------------------------------------------------------
------------
; Initialization BR0/1 and OR0/1 (FLASH)
DATA.set 0FFF00100 %LONG 040000001 /VERIFY
DATA.set 0FFF00104 %LONG 0E0000F52 /VERIFY
DATA.set 0FFF00108 %LONG 060000001 /VERIFY
DATA.set 0FFF0010C %LONG 0E0000F52 /VERIFY
; ab Rev. 200: 0E0000F50

; Initialization BR2/3 and OR2/3 (SDRAM)
DATA.set 0FFF00110 %LONG 000000081 /VERIFY
DATA.set 0FFF00114 %LONG 0E0000B00 /VERIFY
DATA.set 0FFF00118 %LONG 020000081 /VERIFY
DATA.set 0FFF0011C %LONG 0E0000B00 /VERIFY

; ------------------------------------------------------------
------------
; Programming UPMA (for SDRAM)
; ------------------------------------------------------------
------------
; single read (offset 0 in UPMA RAM)
DATA.set 0FFF0017C %LONG 01F0DFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002100 /VERIFY

DATA.set 0FFF0017C %LONG 0EEAFBC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002101 /VERIFY

DATA.set 0FFF0017C %LONG 011AF7C04 /VERIFY
DATA.set 0FFF00168 %LONG 000002102 /VERIFY

DATA.set 0FFF0017C %LONG 0EFBAFC00 /VERIFY
```

©2004 by TQ-Components GmbH

```
DATA.set 0FFF00168 %LONG 000002103 /VERIFY

DATA.set 0FFF0017C %LONG 01FF5FC47 /VERIFY
DATA.set 0FFF00168 %LONG 000002104 /VERIFY

; SDRAM initialisation (offset 5)
DATA.set 0FFF0017C %LONG 01FF5FC34 /VERIFY
DATA.set 0FFF00168 %LONG 000002105 /VERIFY

DATA.set 0FFF0017C %LONG 0EFEABC34 /VERIFY
DATA.set 0FFF00168 %LONG 000002106 /VERIFY

DATA.set 0FFF0017C %LONG 01FB57C35 /VERIFY
DATA.set 0FFF00168 %LONG 000002107 /VERIFY

; burst read (offset 8 in UPMA RAM)
DATA.set 0FFF0017C %LONG 01F0DFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002108 /VERIFY

DATA.set 0FFF0017C %LONG 0EEAFBC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002109 /VERIFY

DATA.set 0FFF0017C %LONG 010AF7C04 /VERIFY
DATA.set 0FFF00168 %LONG 00000210A /VERIFY

DATA.set 0FFF0017C %LONG 0F0AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 00000210B /VERIFY

DATA.set 0FFF0017C %LONG 0F0AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 00000210C /VERIFY

DATA.set 0FFF0017C %LONG 0F1AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 00000210D /VERIFY

DATA.set 0FFF0017C %LONG 0EFBAFC00 /VERIFY
DATA.set 0FFF00168 %LONG 00000210E /VERIFY

DATA.set 0FFF0017C %LONG 01FF5FC47 /VERIFY
DATA.set 0FFF00168 %LONG 00000210F /VERIFY

; single write (offset 18 in UPMA RAM)
DATA.set 0FFF0017C %LONG 01F2DFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002118 /VERIFY

DATA.set 0FFF0017C %LONG 0EEABBC00 /VERIFY
DATA.set 0FFF00168 %LONG 000002119 /VERIFY

DATA.set 0FFF0017C %LONG 001B27C04 /VERIFY
DATA.set 0FFF00168 %LONG 00000211A /VERIFY

DATA.set 0FFF0017C %LONG 01FF5FC47 /VERIFY
DATA.set 0FFF00168 %LONG 00000211B /VERIFY
```

©2004 by TQ-Components GmbH

```
; burst write (offset 20 in UPMA RAM)
DATA.set 0FFF0017C %LONG 01F0DFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002120 /VERIFY

DATA.set 0FFF0017C %LONG 0EEABBC00 /VERIFY
DATA.set 0FFF00168 %LONG 000002121 /VERIFY

DATA.set 0FFF0017C %LONG 010A77C00 /VERIFY
DATA.set 0FFF00168 %LONG 000002122 /VERIFY

DATA.set 0FFF0017C %LONG 0F0AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 000002123 /VERIFY

DATA.set 0FFF0017C %LONG 0F0AFFC00 /VERIFY
DATA.set 0FFF00168 %LONG 000002124 /VERIFY

DATA.set 0FFF0017C %LONG 0E1BAFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002125 /VERIFY

DATA.set 0FFF0017C %LONG 01FF5FC47 /VERIFY
DATA.set 0FFF00168 %LONG 000002126 /VERIFY

; refresh (offset 30 in UPMA RAM)
DATA.set 0FFF0017C %LONG 01FFD7C84 /VERIFY
DATA.set 0FFF00168 %LONG 000002130 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002131 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002132 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC04 /VERIFY
DATA.set 0FFF00168 %LONG 000002133 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC84 /VERIFY
DATA.set 0FFF00168 %LONG 000002134 /VERIFY

DATA.set 0FFF0017C %LONG 0FFFFFC07 /VERIFY
DATA.set 0FFF00168 %LONG 000002135 /VERIFY

; exception (offset 3c in UPMA RAM)
DATA.set 0FFF0017C %LONG 07FFFFC07 /VERIFY
DATA.set 0FFF00168 %LONG 00000213C /VERIFY

; ------------------------------------------------------------
------------
; Refresh and Initialization for SDRAM
; ------------------------------------------------------------
------------
; initialise machine mode a Register (MAMR)
```

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

```
DATA.set 0FFF00170 %LONG 0C3802114 /VERIFY

; initialise memory periodic timer pre-scaler (MPTPR)
; Preliminary pre-scaler for refresh (depends on number of
banks). This value
; is selected for four cycles every 62,4 us with two SDRAM
banks or four
; cycles every 31,2 us with one bank. It will be adjusted
after memory sizing.
DATA.set 0FFF0017A %WORD 01000 /VERIFY

; initialise memory address register (MAR)
DATA.set 0FFF00164 %LONG 000000088 /VERIFY

; precharge-all execute commands via Memory Command Register
at Patch Offset $5
; immediately thereafter from Patch Offset $7 the SDRAM
Initialization
; is done !!
; Banks 0 and 1
DATA.set 0FFF00168 %LONG 080004105 /VERIFY
DATA.set 0FFF00168 %LONG 080006105 /VERIFY

; 2 x 4 times Refresh via Memory Command Register execute at
Patch
; Offset $30
DATA.set 0FFF00168 %LONG 080004130 /VERIFY
DATA.set 0FFF00168 %LONG 080004130 /VERIFY
DATA.set 0FFF00168 %LONG 080006130 /VERIFY
DATA.set 0FFF00168 %LONG 080006130 /VERIFY
```

Illustration 7-1: Initializing SDRAM

The following access types result therefrom:

Single read and burst read

©2004 by TQ-Components GmbH

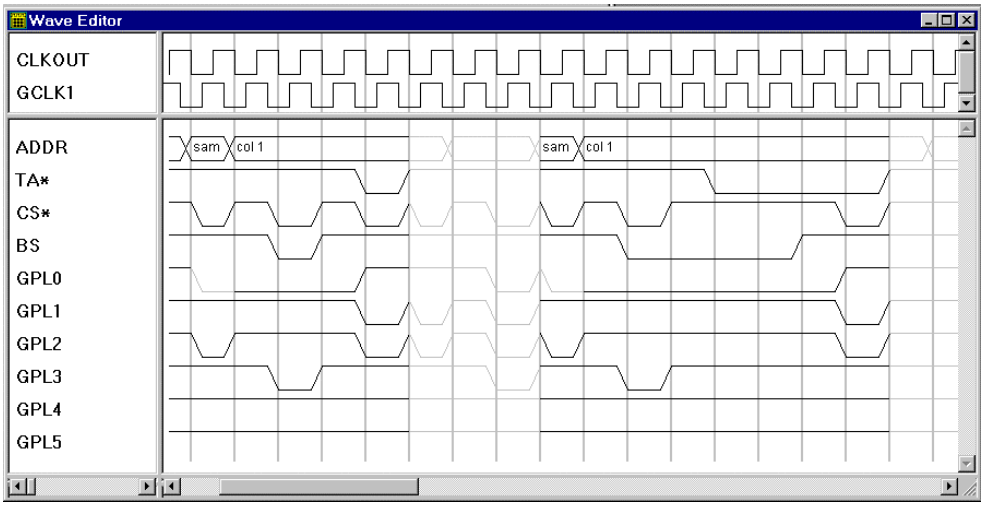


Illustration 7-2: Single read Burst read SDRAM

Single write and burst write

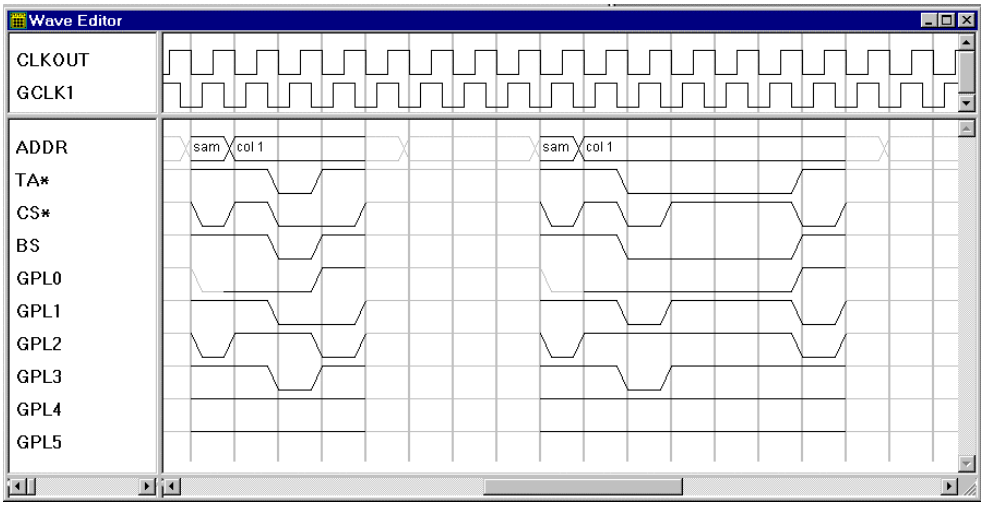


Illustration 7-3: Single write and burst write SDRAM

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

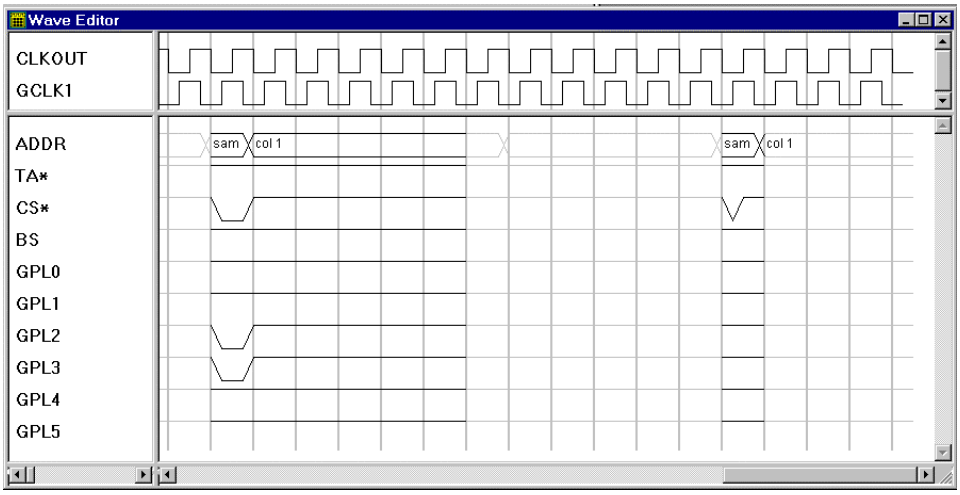


Illustration 7-4: Refresh and Exception SDRAM

7.1.3. Configuration of the CAN Controller

In this example of control (.CMM file for Lauterbach-debugger) both the CAN controllers are configured for the address 0xC0000000. To achieve this the register of the memory controller, the sequencer table of the UPM and the CAN controllers are configured as follows:

```
; Initialising BR2 and OR2 (CAN 1-2)
DATA.SET 0FFF00118 %LONG 0C00004C1 /VERIFY
DATA.SET 0FFF0011C %LONG 0FFFF8500 /VERIFY

; Initialising MBMR for the control of both the CAN
controllers
DATA.SET 0FFF00174 %LONG 00001000 /VERIFY
;DATA.SET 0FFF00174 %LONG 00000000 /VERIFY

; Activate SIUMCR GPL5
; DATA.SET 0FFF00000 %long 001600040 /verify

; Initialising the Micropatch for UPMB/CAN
; single read
DATA.SET 0FFF0017C %LONG 0ffffc004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800100 /VERIFY

DATA.SET 0FFF0017C %LONG 00fffd004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800101 /VERIFY

DATA.SET 0FFF0017C %LONG 00fffc000 /VERIFY
DATA.SET 0FFF00168 %LONG 000800102 /VERIFY

DATA.SET 0FFF0017C %LONG 03fffc004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800103 /VERIFY

DATA.SET 0FFF0017C %LONG 0ffffdc05 /VERIFY
DATA.SET 0FFF00168 %LONG 000800104 /VERIFY
```

©2004 by TQ-Components GmbH

```
; single write
DATA.SET 0FFF0017C %LONG 0fffcc004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800118 /VERIFY

DATA.SET 0FFF0017C %LONG 0cffcd004 /VERIFY
DATA.SET 0FFF00168 %LONG 000800119 /VERIFY

DATA.SET 0FFF0017C %LONG 00ffcc000 /VERIFY
DATA.SET 0FFF00168 %LONG 00080011A /VERIFY

DATA.SET 0FFF0017C %LONG 07ffcc004 /VERIFY
DATA.SET 0FFF00168 %LONG 00080011B /VERIFY

DATA.SET 0FFF0017C %LONG 0fffdcc05 /VERIFY
DATA.SET 0FFF00168 %LONG 00080011C /VERIFY

; disable global Chip Select (CS0#)
DATA.SET 0FFF00100 %LONG 000000000 /VERIFY

; Configuration 82527
; MCLK 8 MHz (@fXTAL = 16 MHz), ISO low speed phys. layer
active
; (-> P2,6 = INT#), CLKOUT active (both CAN controllers)
DATA.SET 0C0000002 %byte 045 /VERIFY
DATA.SET 0C0000102 %byte 045 /VERIFY
```

Illustration 7-5: Configuration of CAN Controllers

This yields the following types of access (the cycles pertaining to those introduced by the wait mechanism are not displayed):

Single read and burst read
Single read and burst read

©2004 by TQ-Components GmbH

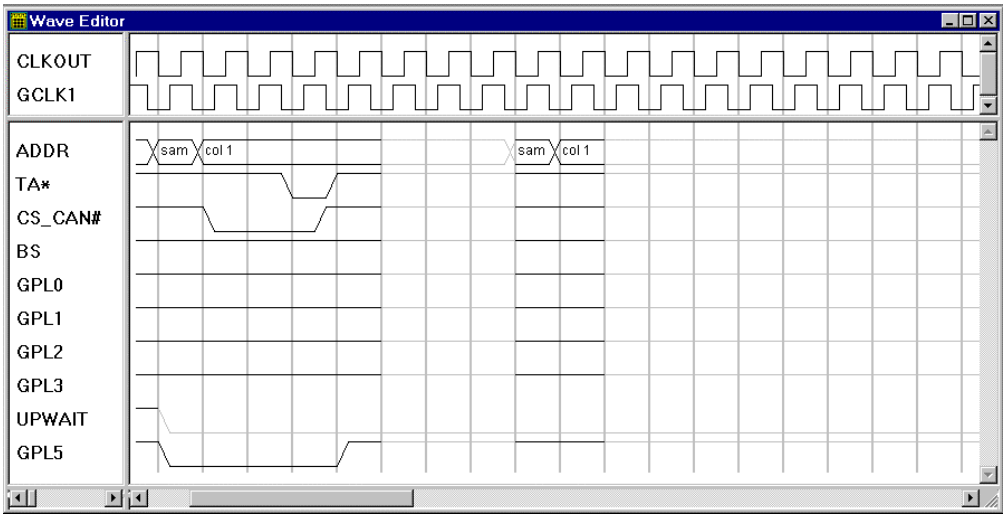


Illustration 7-6: Single read and burst read CAN

Single write and burst write

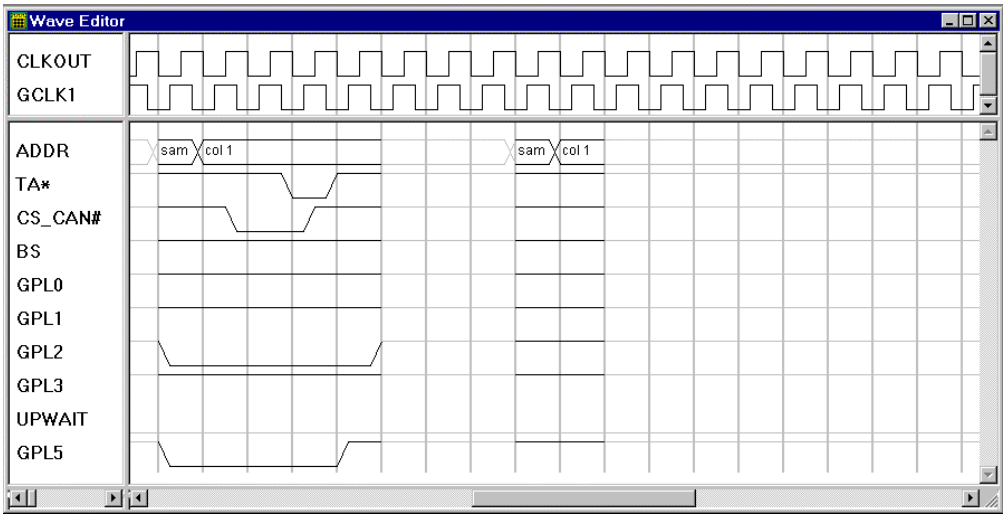


Illustration 7-7: Single write and burst write CAN

©2004 by TQ-Components GmbH

Refresh and Exception

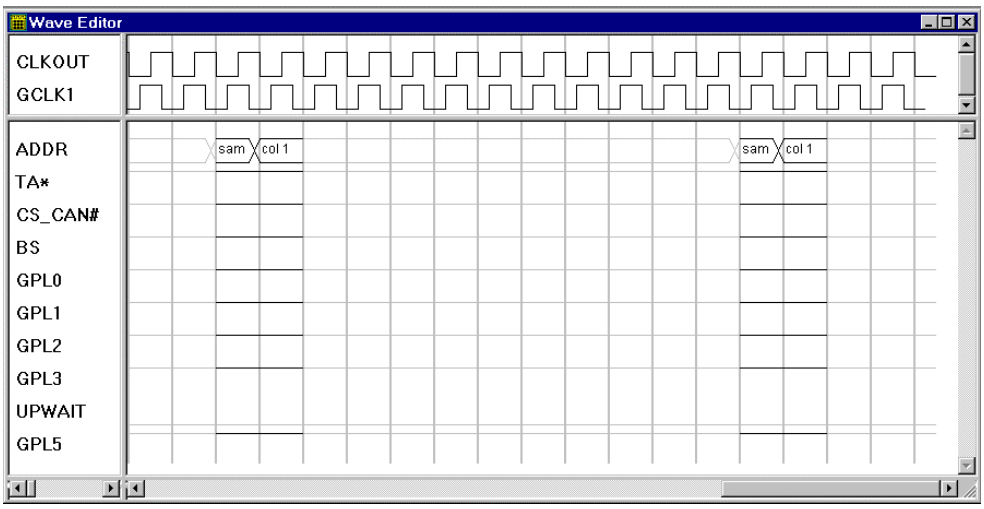


Illustration 7-8: Refresh and Exception CAN

7.2 Tools

7.2.1. Starter Kit STK8xxL

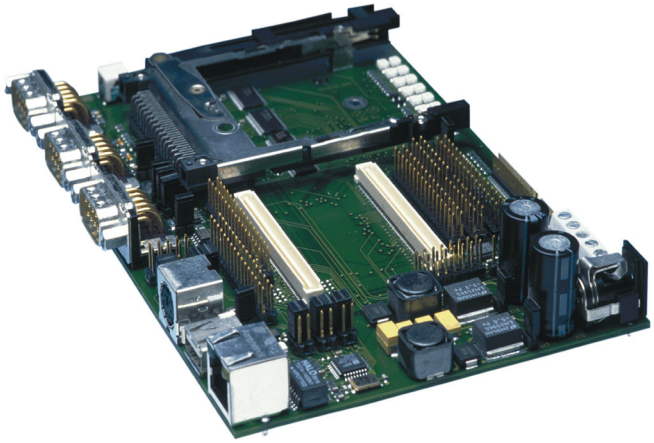


Illustration 7-9: Starter Kit

The STK8xxL can be procured from your sales partner. All modules of the family TQM8xxL and TQM8xxM can be used with the STK8xxL starter kit.

The scope of delivery includes

- Adaptor,
- Download cable,
- Manuals
- Diverse Tool CDs

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH

The following types are available ex-stock:

STK855L-AA	Starter kit STK8xxL with module TQM855LDB0A3-T80	- XPC855TZP80 - 8MB Flash - 16MB SDRAM - No CAN - With regulator - With RS232 driver - 80MHz Clock - Temperature range 0°C...70°C
STK855L-AB	Starter kit STK8xxL with module TQM855LDB0A3-T50	- XPC855TZP50 - 8MB Flash - 16MB SDRAM - No CAN - With regulator - With RS232 driver - 50MHz Clock - Temperature range 0°C...70°C
STK860L-AA	Starter kit STK8xxL with module TQM860LDB0A3-P80	- XPC860PZP80 - 8MB Flash - 16MB SDRAM - no CAN - with regulator - with RS232 driver - 80MHz Clock - Temperature range 0°C...70°C
STK860L-AB	Starter kit STK8xxL with module TQM860LDB0A3-P50	- XPC860PZP50 - 8MB Flash - 16MB SDRAM - No CAN - With regulator - With RS232 driver - 50MHz Clock - Temperature range 0°C...70°C

©2004 by TQ-Components GmbH

STK860L-AD	Starter kit STK8xxL with module TQM860LDDBA3-P50	- XPC860PZP50 - 8MB Flash - 64MB SDRAM - CAN Controller 1 and 2 fitted - With regulator - With RS232 driver - 50MHz Clock - Temperature range 0°C...70°C
STK862L-AA	Starter kit STK8xxL with module TQM862LDB0A3-SR80	- XPC860SRZP80 - 8MB Flash - 16MB SDRAM - No CAN - With regulator - With RS232 driver - 80MHz Clock - Temperature range 0°C...70°C

Illustration 7-10: Standard types of the starter kit

7.2.2. Module Extraction Tool MOZI8xxL

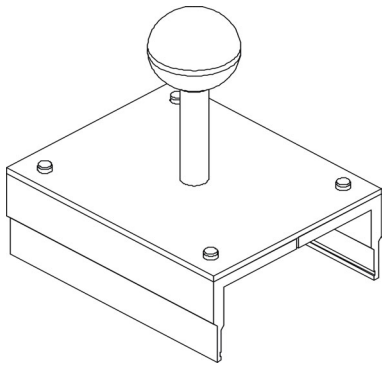


Illustration 7-11: Module Extraction Tool

	To ensure elegant removal (plug-out) of the module from the motherboard making use of the extraction tool MOZI8xxL, which is supplied along with the starter kit, is mandatory.

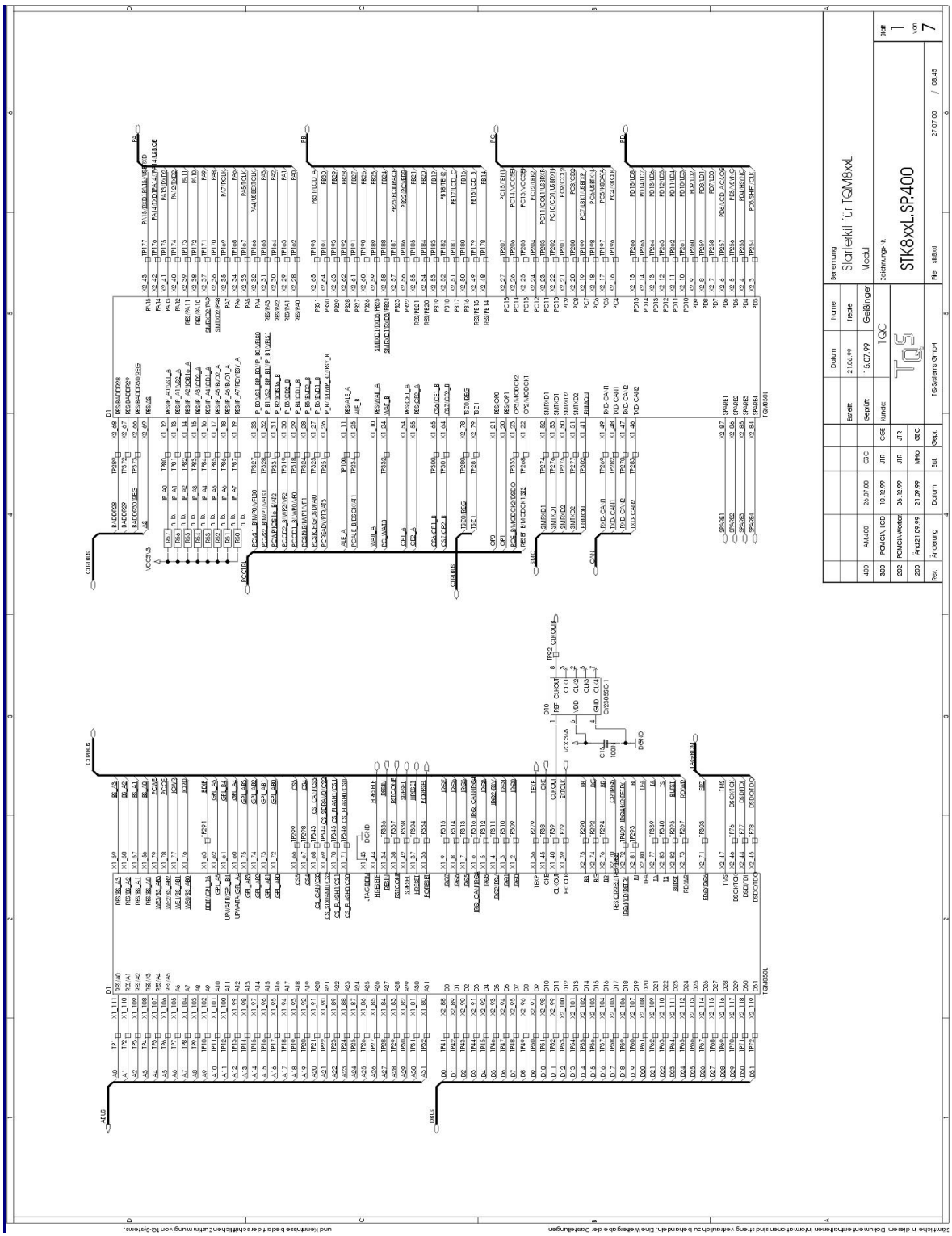
The MOZI8xxL can be procured from your sales partner.

TQM8xxL.HWM.0300.doc

©2004 by TQ-Components GmbH

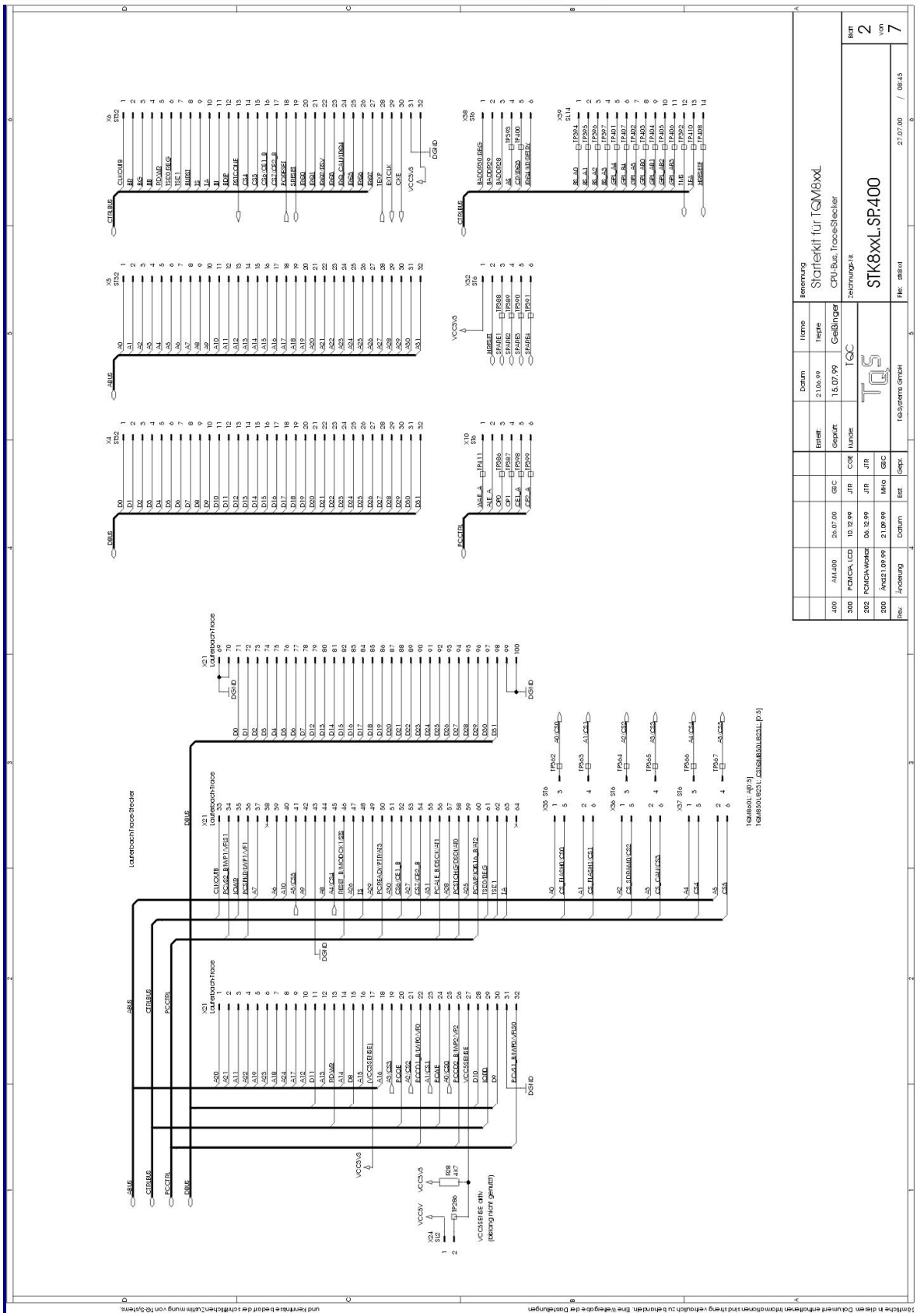
7.3 Circuit Diagrams

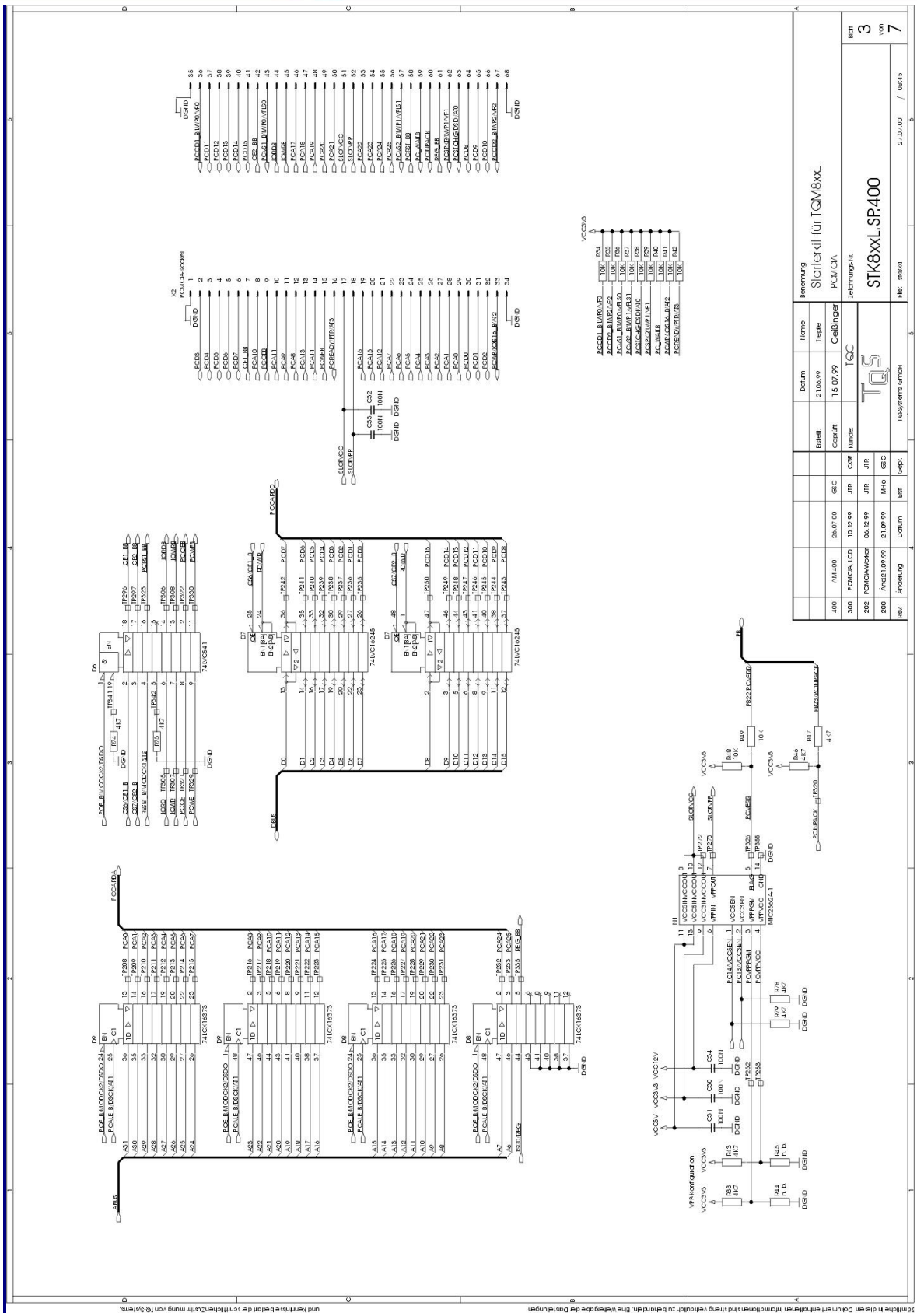
7.3.1. Starter Kit



©2004 by TQ-Components GmbH

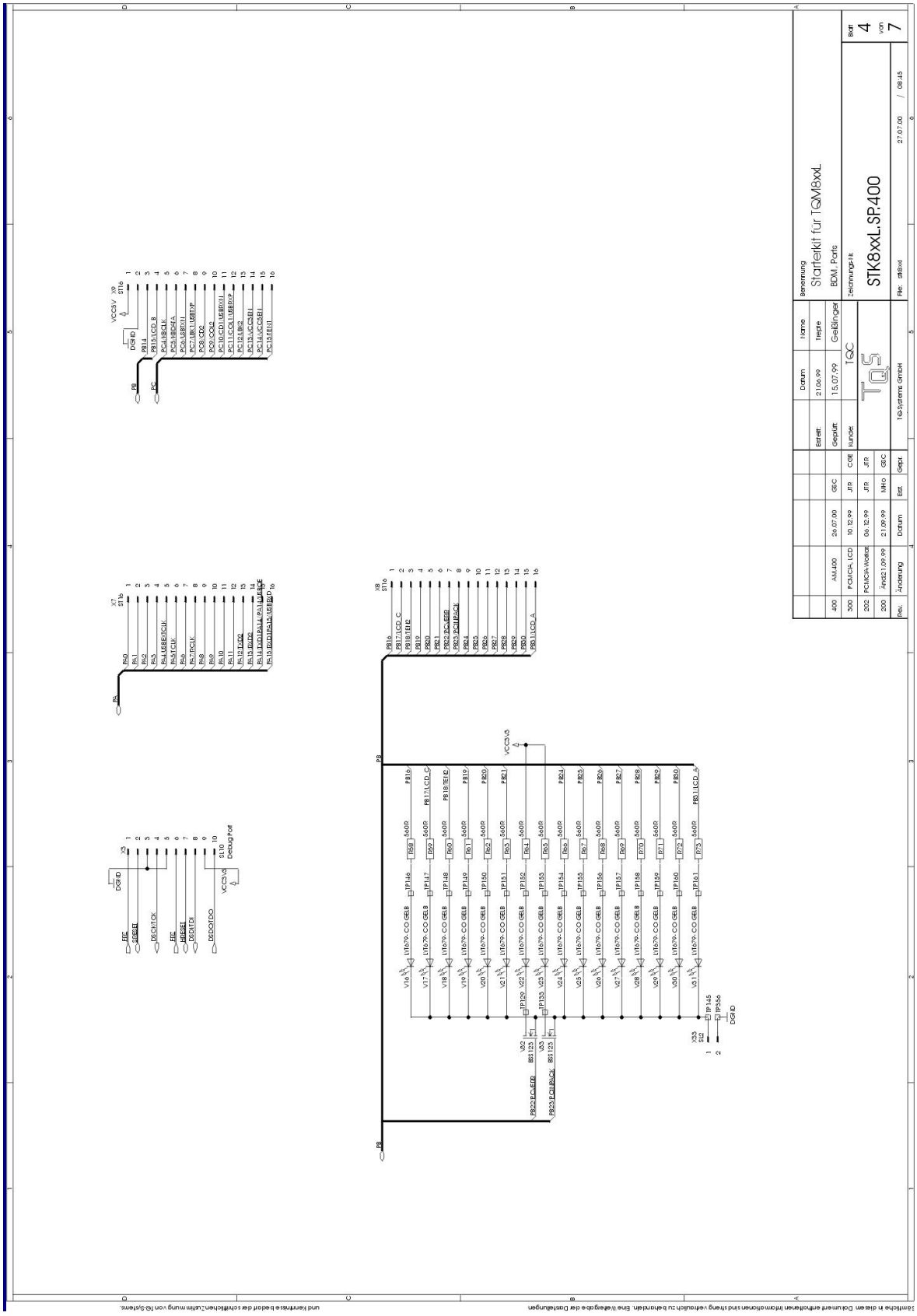
©2004 by TQ-Components GmbH

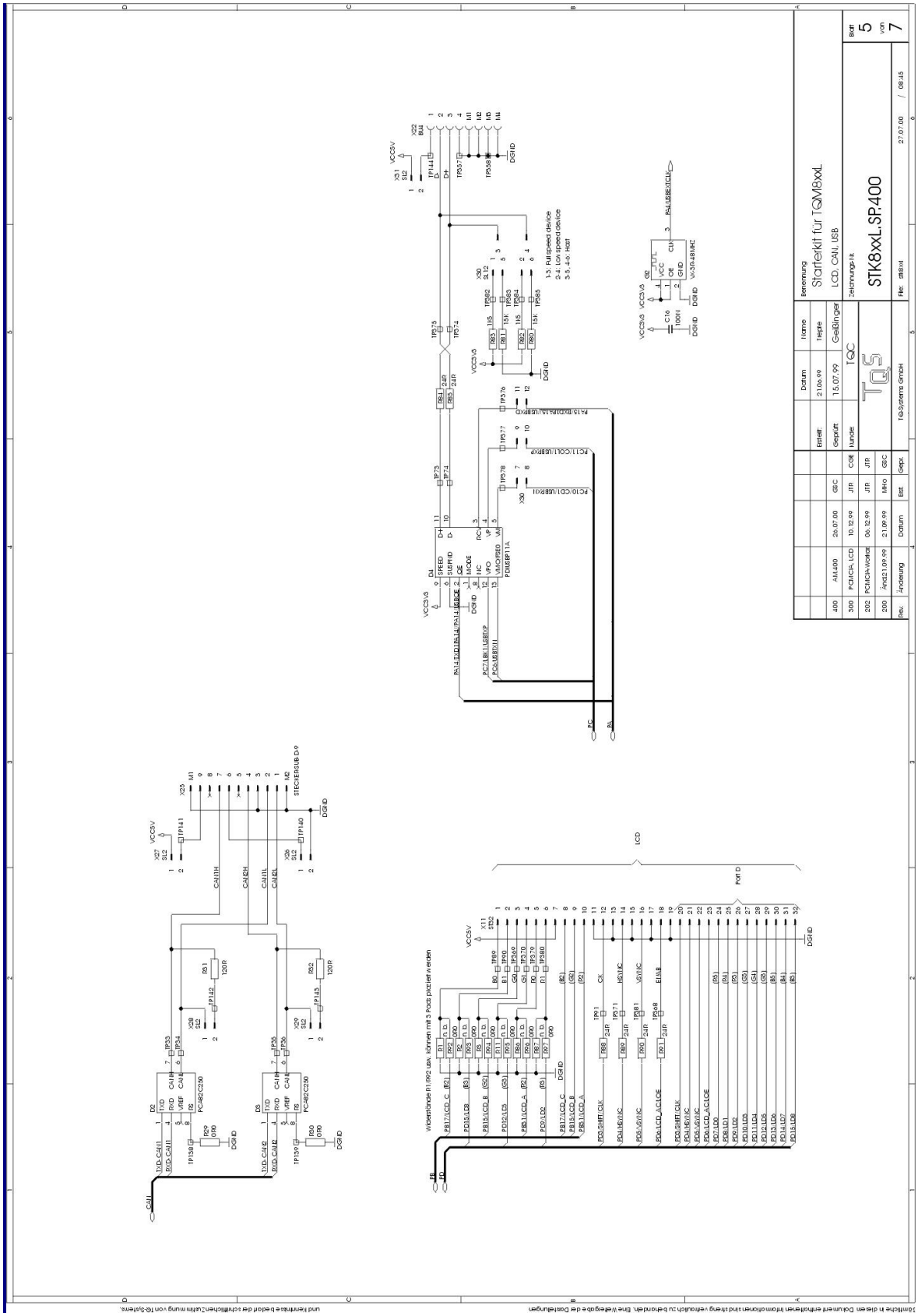




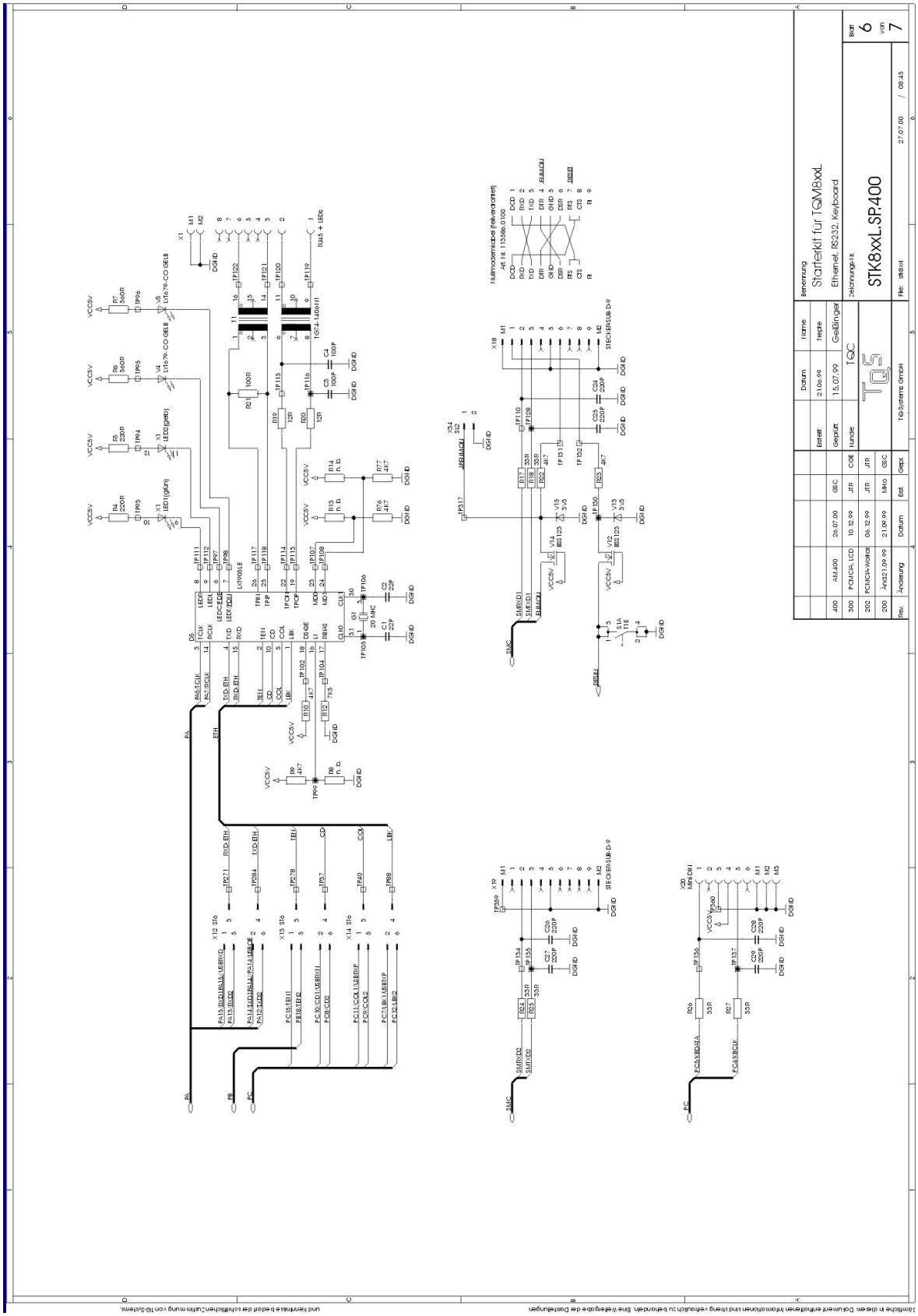
©2004 by TQ-Components GmbH

©2004 by TQ-Components GmbH

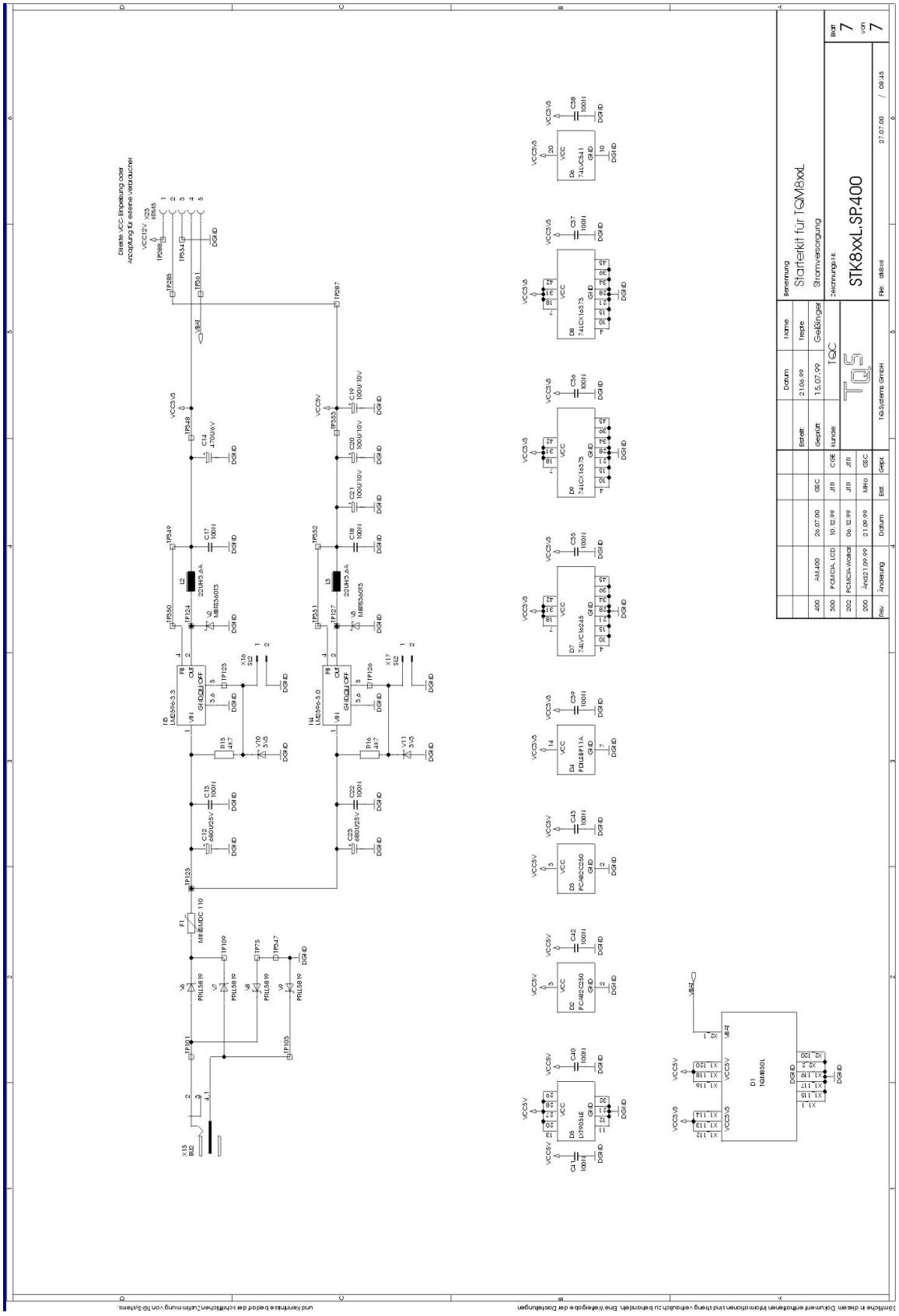




©2004 by TQ-Components GmbH

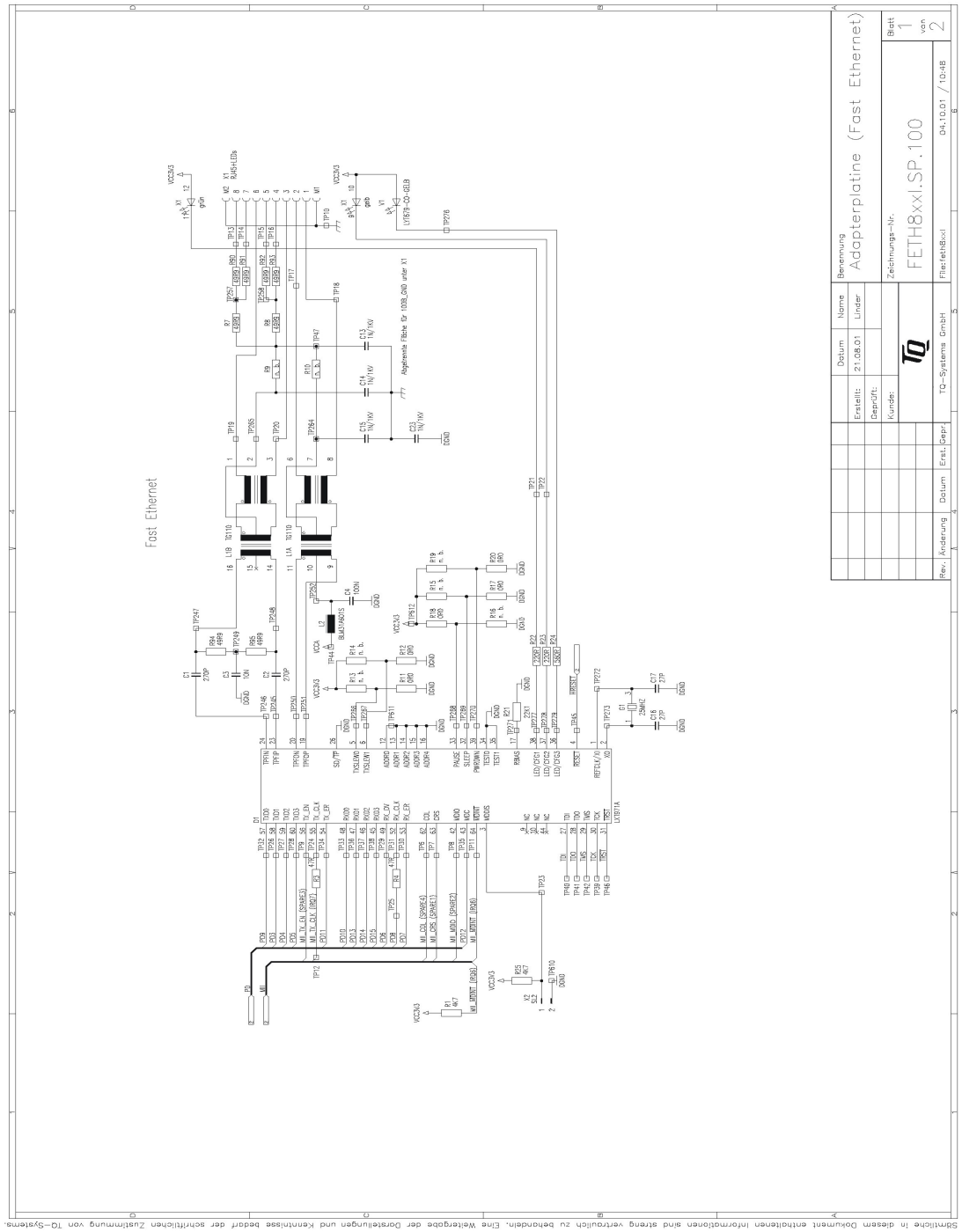


©2004 by TQ-Components GmbH

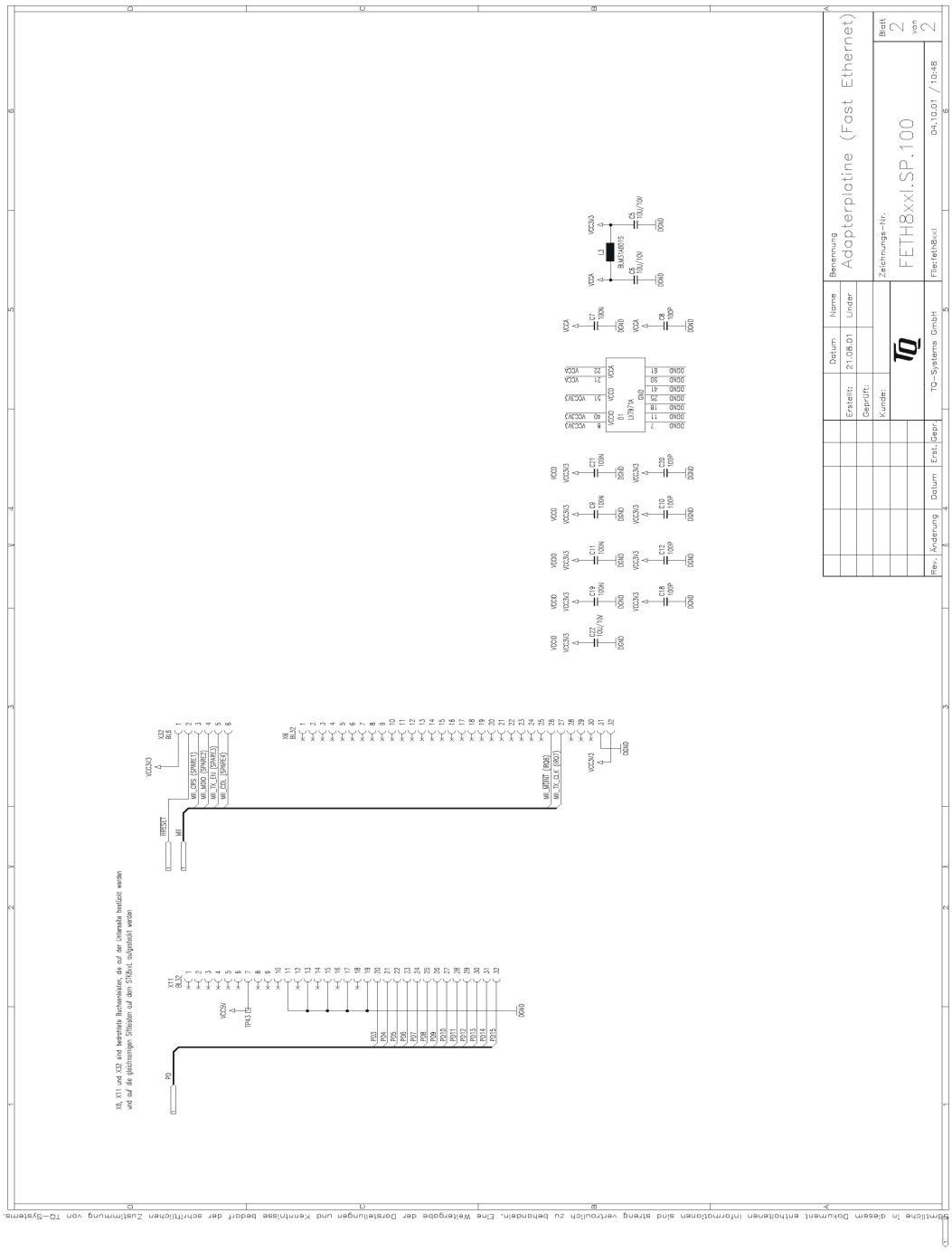


©2004 by TQ-Components GmbH

7.3.2. FETH8xxL



©2004 by TQ-Components GmbH



©2004 by TQ-Components GmbH

7.4 Literature

[1] MPC860 PowerQUICC™ User's Manual
MPC860UM/AD Rev. 1, 07/98

[2] Errata to MPC860 PowerQUICC™ User 's Manual Rev.1
MPC860UMAD/D, Rev.2,6/2001

[3] MPC855T User's Manual
Integrated Communications Microprocessor
MPC855TUM/D Rev. 0, 2/2001

[4] AM29LV160D
16 Megabit (2 M x 8 bit/1 M x 16-Bit) CMOS 3.0 Volt-only Boot Sector Flash Memory
Publication #22358 Rev. A Amendment /+1, Issue Date April 19, 1999

[5] 256 MB: x4, x8, x16 SDRAM
256MSDRAM_C.p65 – Rev. C; Pub. 4/01

[6] 82527 Serial Communications Controller
Controller Area Network Protocol
Order Number 272250-006, December 1995

[7] Intel 1999 Packaging Data handbook

[8] MAX3222/MAX3232/MAX3237/MAX3241
3,0V to 5,5V, Low-power, up to 1Mbps, True RS-232 Transceivers Using Four 0,1µF External Capacitors
19-0273; Rev 5; 3/99

[9] MAX814/MAX815/MAX816
±1 % Accuracy, Low-power, +3V and +5V µP Supervisory Circuits
19-0412, Rev 0, 6/95

[10] Anla Technology Co., Ltd.
EMC EMI Component SMD

[11] Product Specification 108-5390
AMP FH 0,8 mm Pitch board-to-board connector
AMP J-552 (Rev. Mar 91)

[12] Life cycle and reliability calculation
Working instructions QMAA0704A05 Rev. 109, TQ-Systems GmbH

TQM8xxL.HWM.0300.doc
©2004 by TQ-Components GmbH